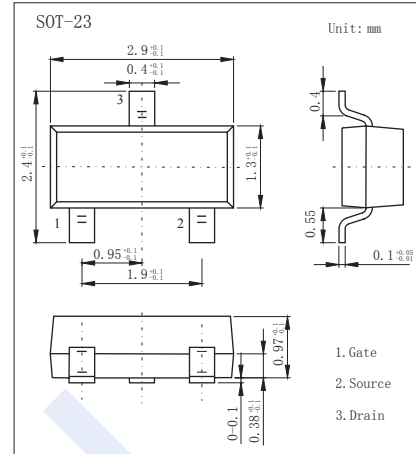
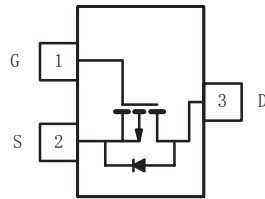


## P-Channel Enhancement MOSFET

### SI2333CDS (KI2333CDS)

#### ■ Features

- $V_{DS}$  (V) = -12V
- $I_D$  = -5.1A ( $V_{GS}$  = -4.5V)
- $R_{DS(ON)}$  < 35m $\Omega$  ( $V_{GS}$  = -4.5V)
- $R_{DS(ON)}$  < 45m $\Omega$  ( $V_{GS}$  = -2.5V)
- $R_{DS(ON)}$  < 59m $\Omega$  ( $V_{GS}$  = -1.8V)



#### ■ Absolute Maximum Ratings $T_a = 25^\circ\text{C}$

Parameter	Symbol	5 sec	Steady State	Unit
Drain-Source Voltage	$V_{DS}$	-12		V
Gate-Source Voltage	$V_{GS}$	$\pm 8$		
Continuous Drain Current	$I_D$	$T_a = 25^\circ\text{C}$	-7.1	A
		$T_a = 70^\circ\text{C}$	-5.7	
Pulsed Drain Current	$I_{DM}$	-20		
Power Dissipation	$P_D$	$T_a = 25^\circ\text{C}$	2.5	W
		$T_a = 70^\circ\text{C}$	1.6	
Thermal Resistance.Junction- to-Ambient	$R_{thJA}$	100		$^\circ\text{C}/\text{W}$
Thermal Resistance.Junction- to-Foot	$R_{thJF}$	50		
Junction Temperature	$T_J$	150		$^\circ\text{C}$
Storage Temperature Range	$T_{stg}$	-55 to 150		

## P-Channel Enhancement MOSFET

### SI2333CDS (KI2333CDS)

#### ■ Electrical Characteristics Ta = 25°C

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V <sub>DSS</sub>	I <sub>D</sub> =-250 μA, V <sub>GS</sub> =0V	-12			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =-12V, V <sub>GS</sub> =0V			-1	μA
		V <sub>DS</sub> =-12V, V <sub>GS</sub> =0V, T <sub>J</sub> =55°C			-10	
Gate-Body leakage current	I <sub>GSS</sub>	V <sub>DS</sub> =0V, V <sub>GS</sub> =±8V			±100	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> I <sub>D</sub> =-250 μA	-0.4		-1	V
Static Drain-Source On-Resistance *1	R <sub>DS(on)</sub>	V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-5.1A		28.5	35	mΩ
		V <sub>GS</sub> =-2.5V, I <sub>D</sub> =-4.5A		36	45	
		V <sub>GS</sub> =-1.8V, I <sub>D</sub> =-2.0A		46	59	
On state drain current *1	I <sub>D(ON)</sub>	V <sub>GS</sub> =-4.5V, V <sub>DS</sub> =-5V	-20			A
Forward Transconductance *1	g <sub>FS</sub>	V <sub>DS</sub> =-5V, I <sub>D</sub> =-1.9A		1.6		S
Gate Resistance	R <sub>g</sub>	f=1.0MHz		4.0		Ω
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> =0V, V <sub>DS</sub> =-6V, f=1MHz		1225		pF
Output Capacitance	C <sub>oss</sub>			315		
Reverse Transfer Capacitance	C <sub>rss</sub>			260		
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> =-4.5V, V <sub>DS</sub> =-6V, I <sub>D</sub> =-5.1A		15	25	nC
				9	15	
Gate Source Charge	Q <sub>gs</sub>	V <sub>GS</sub> =-2.5V, V <sub>DS</sub> =-6V, I <sub>D</sub> =-5.1A		1.9		
Gate Drain Charge	Q <sub>gd</sub>			3.8		
Turn-On DelayTime	t <sub>d(on)</sub>	V <sub>GS</sub> =-4.5V, V <sub>DS</sub> =-6V, R <sub>L</sub> =6Ω, R <sub>GEN</sub> =1Ω  I <sub>D</sub> =-1.0A		13	20	ns
Turn-On Rise Time	t <sub>r</sub>			35	60	
Turn-Off DelayTime	t <sub>d(off)</sub>			45	70	
Turn-Off Fall Time	t <sub>f</sub>			12	20	
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>	I <sub>F</sub> = 1.0 A, di/dt = 100 A/ us, T <sub>J</sub> =25°C		20	40	nC
Body Diode Reverse Recovery Time	t <sub>rr</sub>			32	50	ns
Reverse Recovery Fall Time	t <sub>a</sub>			16		
Reverse Recovery Rise Time	t <sub>b</sub>			16		
Maximum Body-Diode Continuous Current	I <sub>S</sub>	T <sub>C</sub> =25°C			-1.0	A
Pulse Diode Forward Current *1	I <sub>SM</sub>				-20	
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =-1.0A, V <sub>GS</sub> =0V		-0.7	-1.2	V

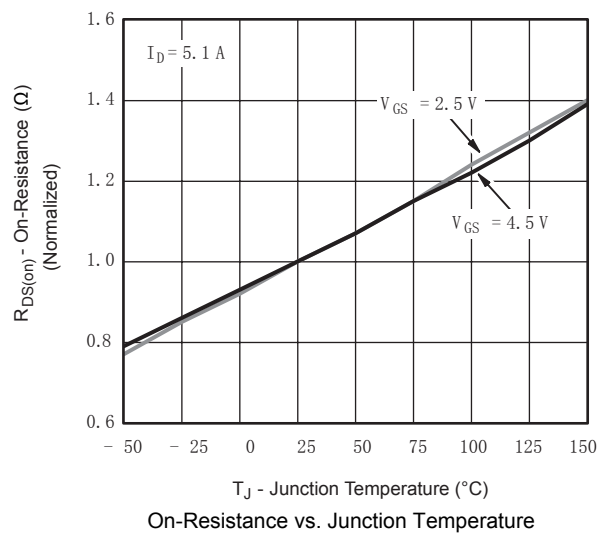
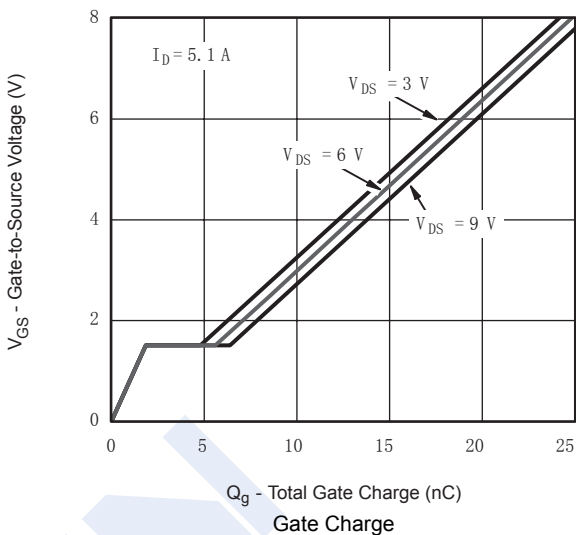
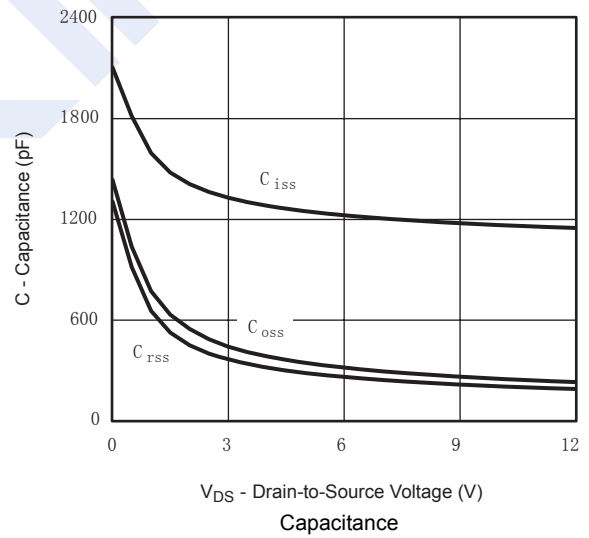
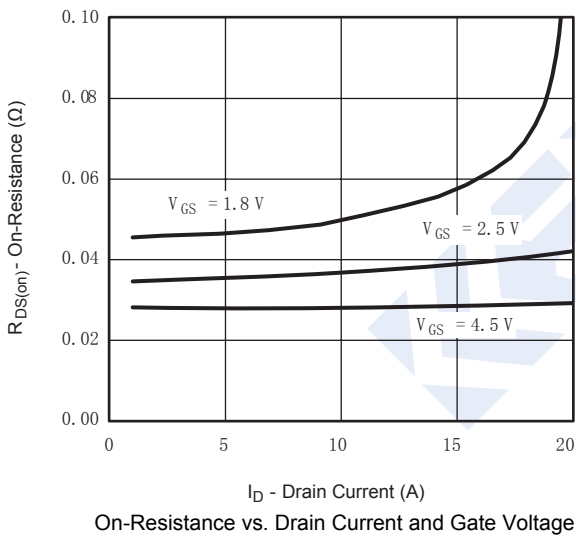
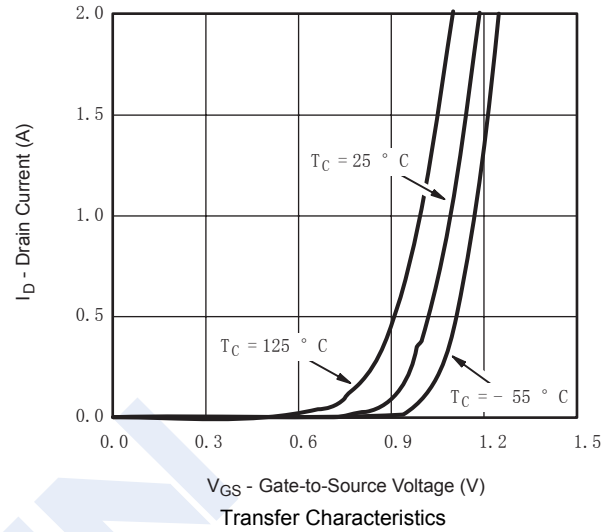
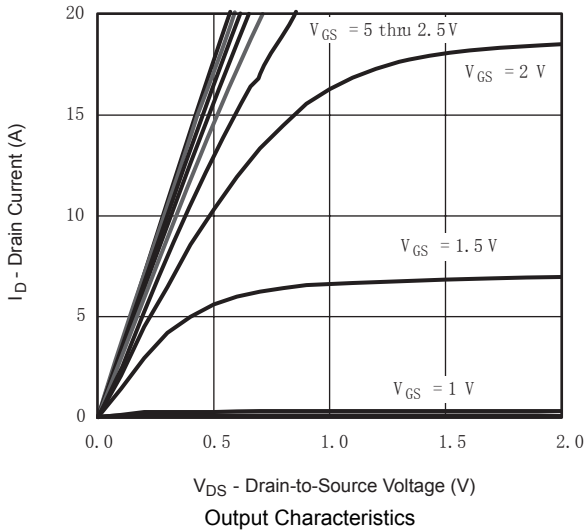
\*1Pulse test: PW ≤ 300us duty cycle ≤ 2%.

#### ■ Marking

Marking	O3*
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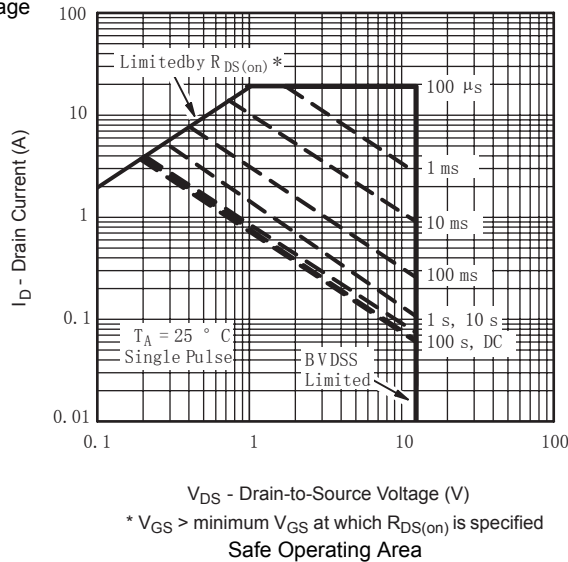
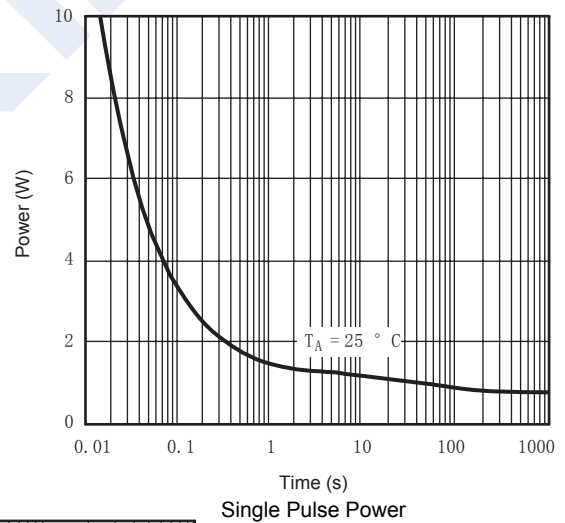
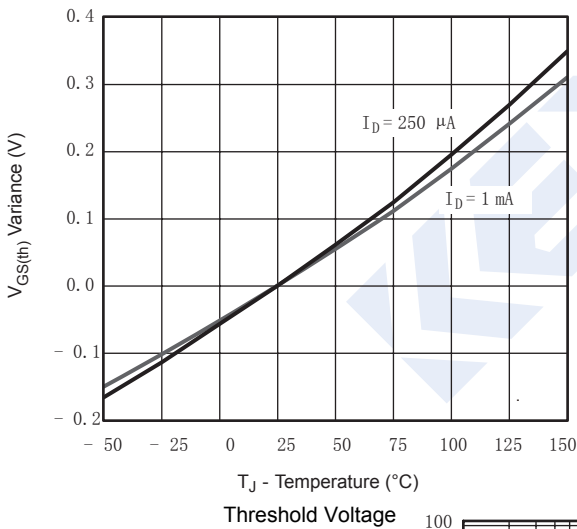
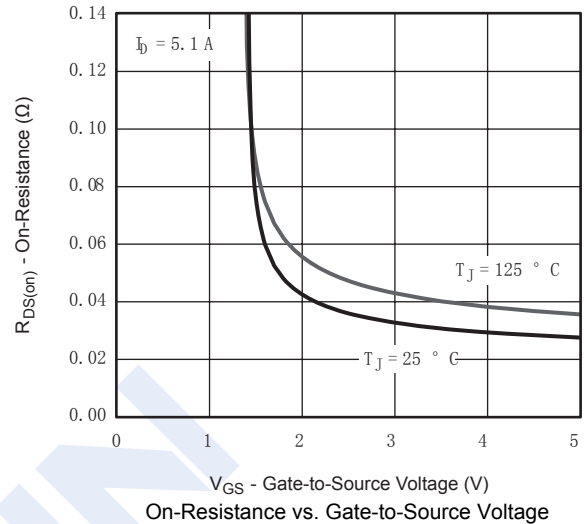
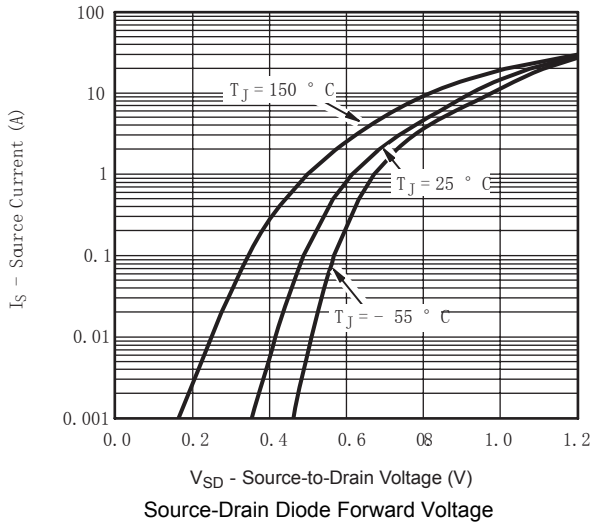
## P-Channel Enhancement MOSFET SI2333CDS (KI2333CDS)

■ Typical Characteristics



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