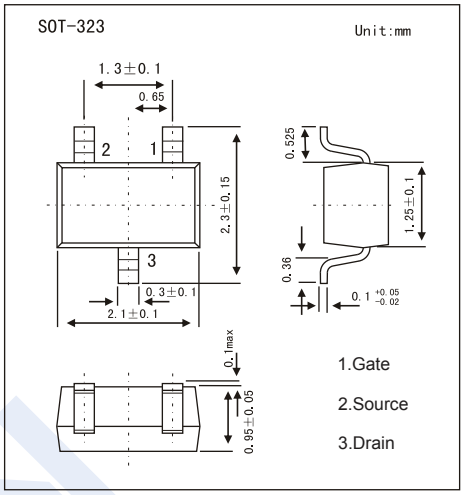
P-Channel MOSFET

AO7401 (KO7401)



■ Features

- V_{DS} -30V
- I_D (at V_{GS}=-10V) -1.4A
- $R_{DS(ON)}$ (at V_{GS} =-10V) < 115mΩ
- $R_{DS(ON)}$ (at V_{GS} =-4.5V) < 140mΩ
- $R_{DS(ON)}$ (at V_{GS} =-2.5V) < 200mΩ

■ Absolute Maximum Ratings T_A = 25℃ unless otherwise noted.

Parameter		Symbol	Rating	Unit
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	±12	
Continuous Drain Current	T_A=25℃	I_D	-1.4	A
	T_A=70℃		-1.0	
Pulsed Drain Current [C]		I_{DM}	-10	
Power Dissipation [B]	T_A=25℃	P_D	0.35	W
	T_A=70℃		0.22	
Thermal Resistance.Junction- to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	360	℃/W
Thermal Resistance.Junction- to-Ambient [A D]	Steady-State		425	
Thermal Resistance.Junction- to-Lead	Steady-State	$R_{\theta JL}$	320	
Junction Temperature		T_J	150	℃
Storage Temperature Range		T_{stg}	-55 to 150	

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on $T_{J(MAX)}$=150°C, using ≤ 10s junction-to-ambient thermal resistance.

C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150°C. Ratings are based on low frequency and duty cycles to keep initial T_J=25°C.

D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to lead $R_{\theta JL}$ and lead to ambient.

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■ Electrical Characteristics (T_J = 25℃ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = -250μA, V_{GS} = 0V	-30			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}= -30V, V_{GS} = 0V			-1	μA
		V_{DS}= -30V, V_{GS} = 0V, T_J = 55℃			-5	
Gate-Body Leakage Current	I_{GSS}	V_{DS} = 0V, V_{GS} = ±12V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS} , I_D = -250μA	-0.6		-1.4	V
On state drain current	$I_{D(ON)}$	V_{GS}=-10V, V_{DS}=-5V	-10			A
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS} = -10V, I_D = -1.4A			115	mΩ
		V_{GS} = -10V, I_D = -1.4A, T_J = 125℃			160	
		V_{GS} = -4.5V, I_D = -1.2A			140	
		V_{GS} = -2.5V, I_D = -1A			200	
Forward Transconductance	g_{FS}	V_{DS} = -5V, I_D = -1.4A		6		S
Input Capacitance	C_{iss}	V_{GS}=0V, V_{DS} = -15V, f = 1MHz		260	315	pF
Output Capacitance	C_{oss}			37		
Reverse Transfer Capacitance	C_{rss}			20		
Gate resistance	Rg	V_{GS}=0V, V_{DS}=0V, f=1MHz	4		12	Ω
Total Gate Charge	Q_g(10V)	V_{DS} = -15V, I_D = -1.4A V_{GS} = -10V		5.9	7.2	nC
	Q_g(4.5V)			2.8	3.5	
Gate Source Charge	Q_{gs}			0.7		
Gate Drain Charge	Q_{gd}			1		
Turn-On DelayTime	$t_{d(on)}$	V_{GS} = -10V, V_{DS} = -15V, R_L = 10Ω, R_{GEN} = 3Ω		6		ns
Turn-On Rise Time	t_r			3.5		
Turn-Off DelayTime	$t_{d(off)}$			20		
Turn-Off Fall Time	t_f			5		
Body Diode Reverse Recovery Time	t_{rr}	I_F= -1.4A, dI/dt= 100A/μs		11.5	15	
Body Diode Reverse Recovery Charge	Q_{rr}	I_F= -1.4A, dI/dt= 100A/μs		4.5		nC
Maximum Body-Diode Continuous Current	I_S				-0.5	A
Diode Forward Voltage	V_{SD}	I_S = -1 A,V_{GS} = 0V			-1	V

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, assuming a maximum junction temperature of $T_{J(MAX)}$=150°C. The SOA curve provides a single pulse rating.

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■ Typical Electrical and Thermal Characterisitics

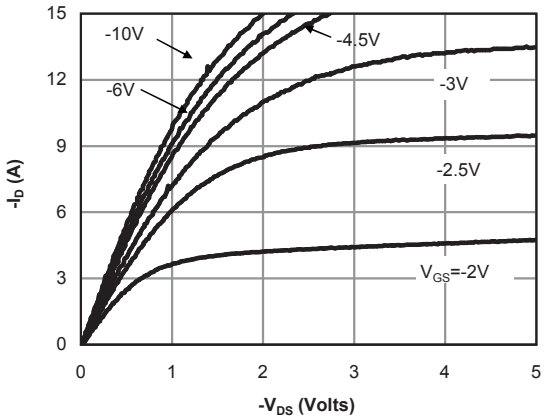

Fig 1: On-Region Characteristics (Note E)

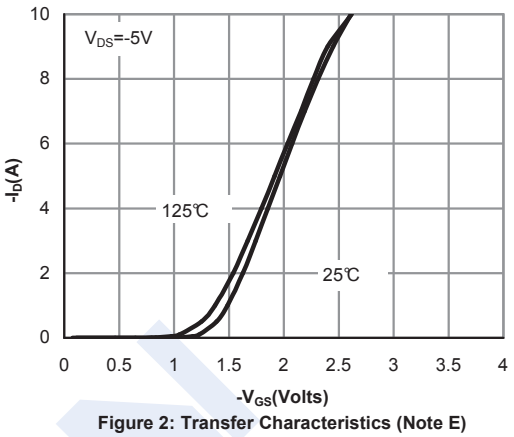

Figure 2: Transfer Characteristics (Note E)

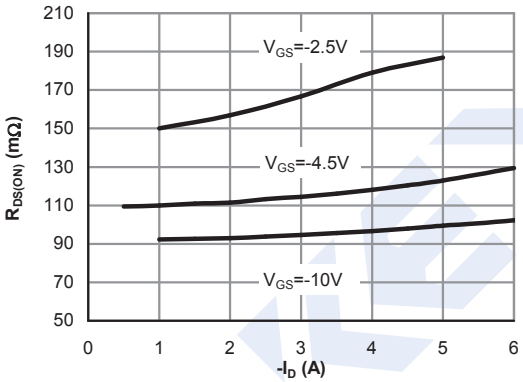

Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

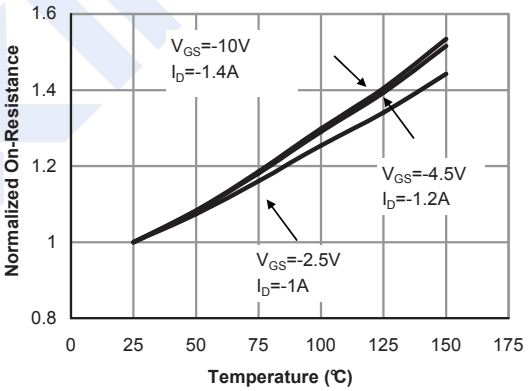

Figure 4: On-Resistance vs. Junction Temperature (Note E)

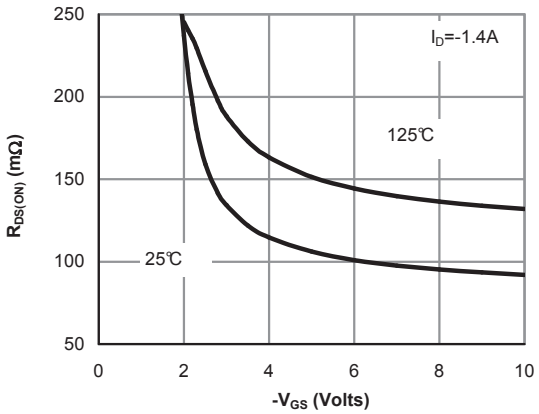

Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

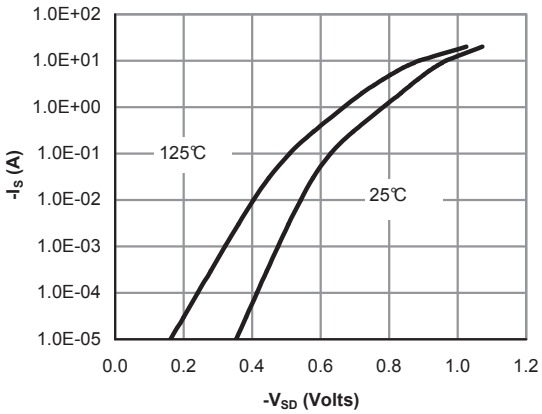

Figure 6: Body-Diode Characteristics (Note E)

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■ Typical Electrical and Thermal Characterisitics

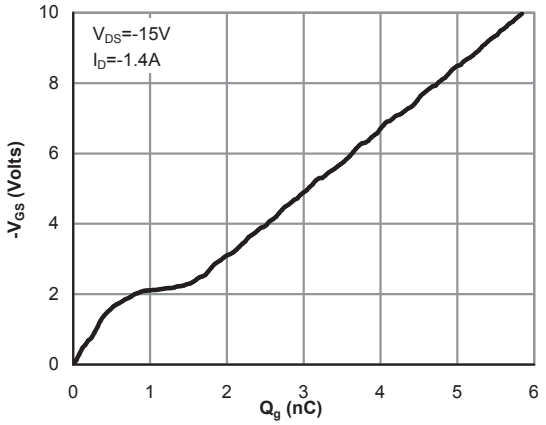

Figure 7: Gate-Charge Characteristics

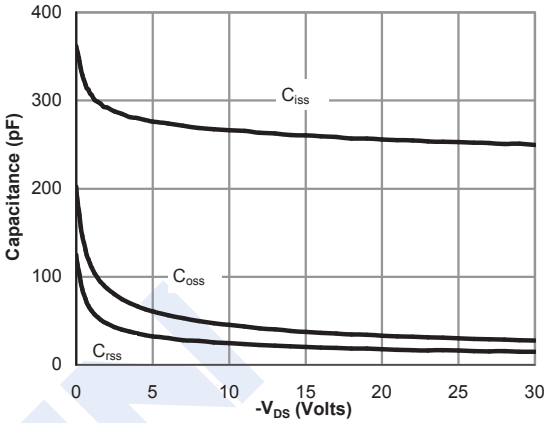

Figure 8: Capacitance Characteristics

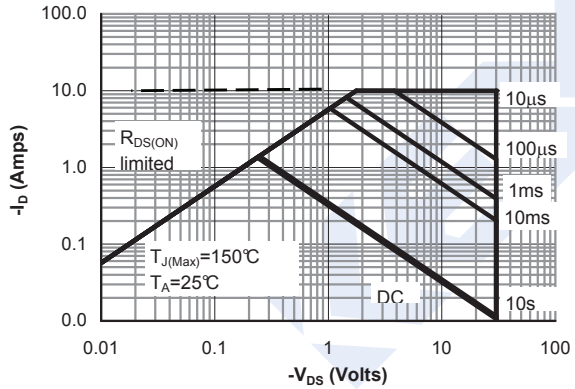

Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

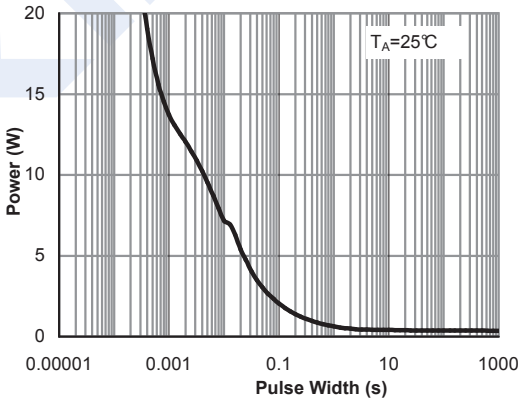

Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

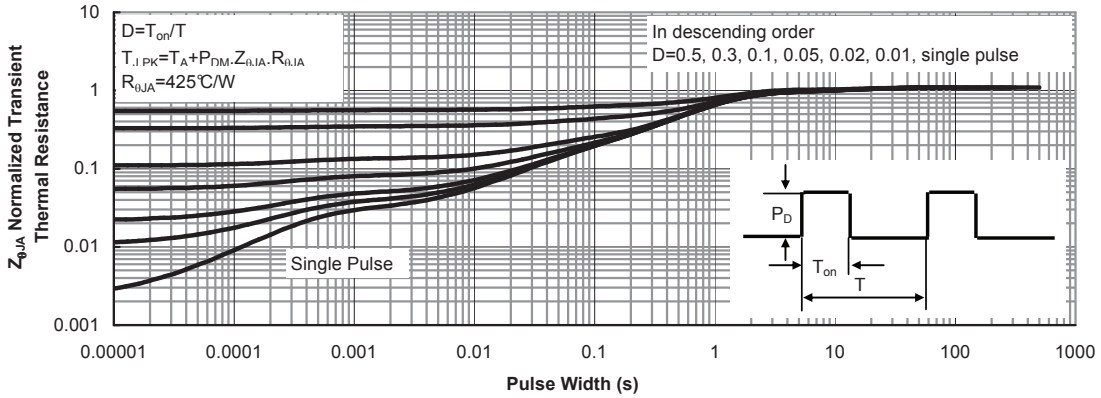

Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

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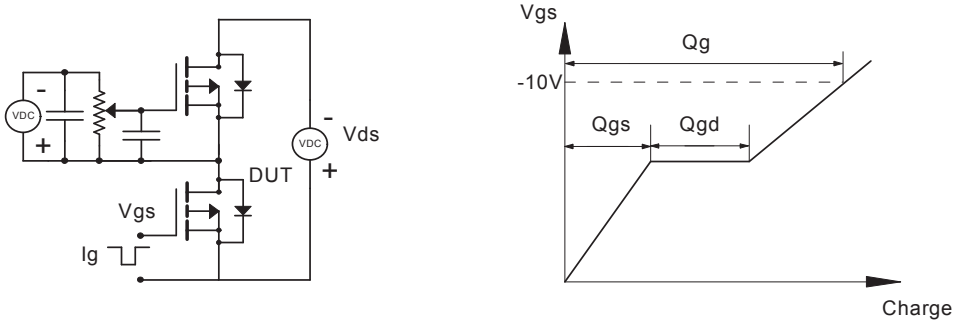
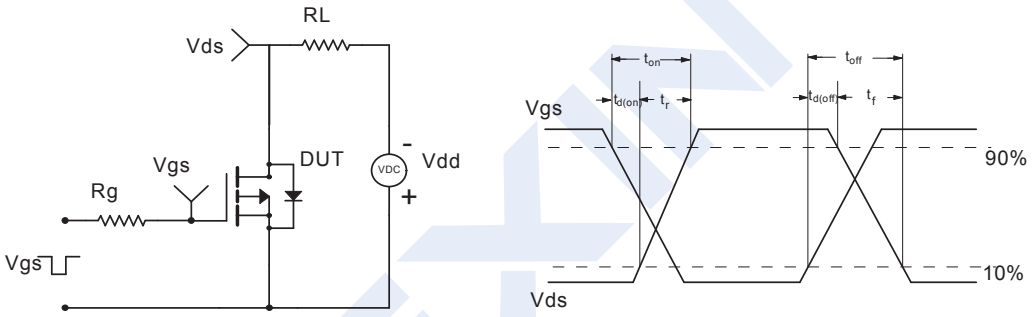
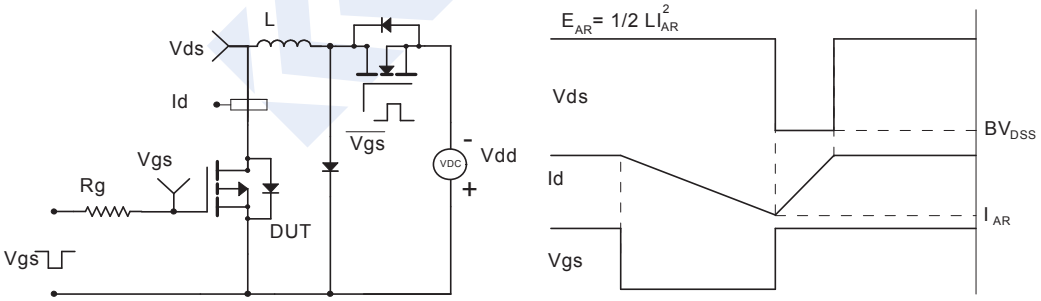
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms