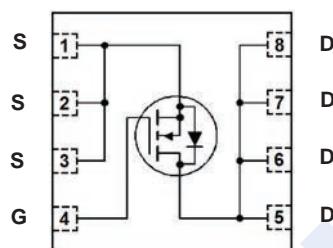


N-Channel MOSFET

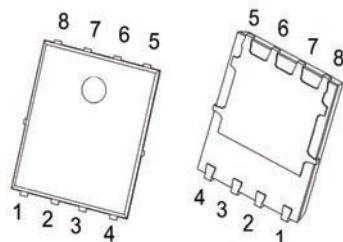
2KK5115DFN

■ Features

- V_{DS} (V) = 60 V
- $I_{D\text{MAX}} = 80$ A
- $R_{DS(\text{ON})} < 7.5\text{m}\Omega$ @ $V_{GS}=10\text{V}$
- $R_{DS(\text{ON})} < 9.5\text{m}\Omega$ @ $V_{GS}=4.5\text{V}$



DFN5x6-8

■ Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ unless otherwise noted)

| Parameter | Symbol | Rating | Unit |
|---|-----------------|------------|---------------------------|
| Drain-Source Voltage | V_{DS} | 60 | V |
| Gate-Source Voltage | V_{GS} | ± 20 | |
| Continuous Drain Current | I_D | 80 | A |
| | | 51 | |
| Continuous Drain Current | I_D | 10 | |
| | | 8 | |
| Pulsed Drain Current (Note 1) | I_{DM} | 200 | |
| Diode Continuous Forward Current | I_S | 25 | |
| Avalanche Current, Single pulse ($L=0.5\text{mH}$) (Note 2) | I_{AS} | 20 | |
| Avalanche Energy, Single pulse ($L=0.5\text{mH}$) (Note 2) | E_{AS} | 100 | mJ |
| Power Dissipation | P_D | 52 | W |
| | | 20.8 | |
| Power Dissipation | P_D | 2 | |
| | | 1.3 | |
| Thermal Resistance.Junction- to-Case | $R_{\theta JC}$ | 2.4 | $^\circ\text{C}/\text{W}$ |
| Thermal Resistance.Junction- to-Ambient (Note 3) | $R_{\theta JA}$ | 25 | |
| | | 60 | |
| Junction Temperature | T_J | 150 | $^\circ\text{C}$ |
| Storage Temperature Range | T_{Stg} | -55 to 150 | |

Notes 1. Pulse width limited by max. junction temperature.

2. UIS tested and pulse width limited by maximum junction temperature 150°C (initial temperature $T_j=25^\circ\text{C}$).

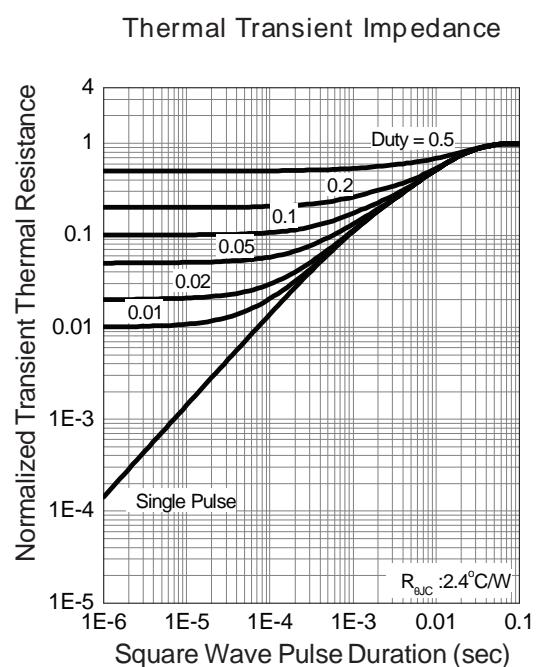
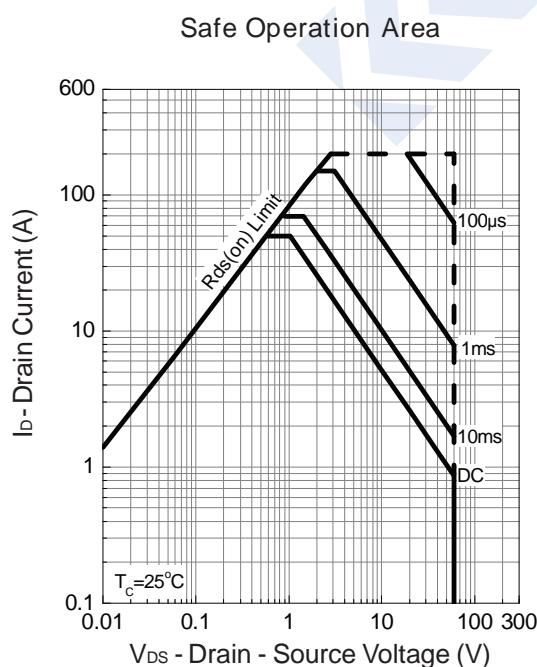
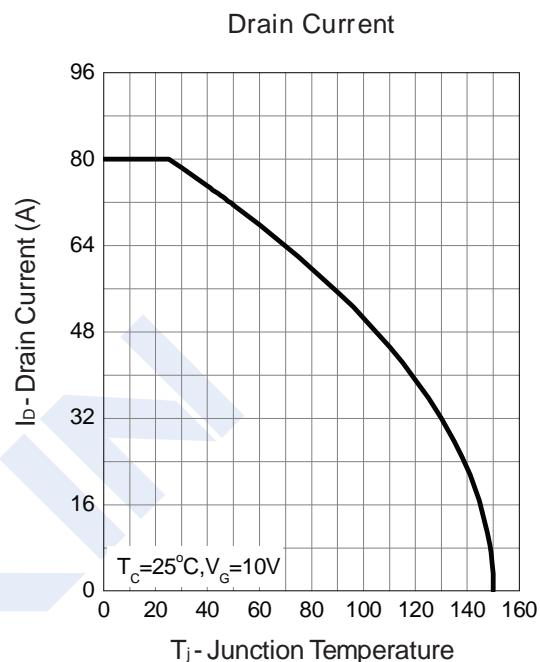
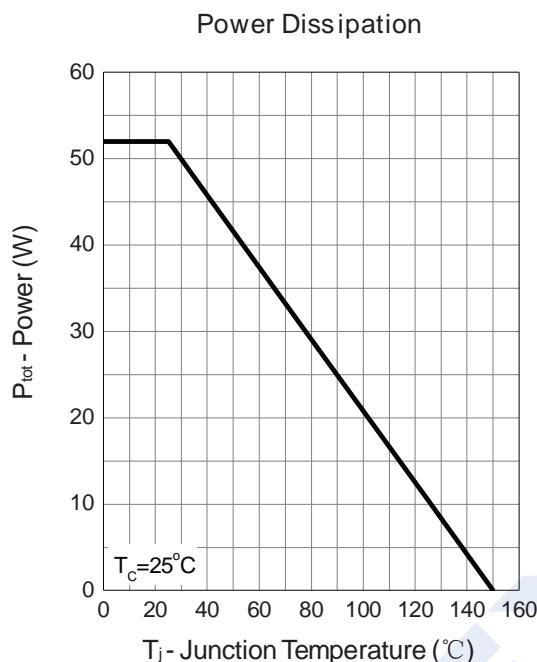
3. Surface Mounted on 1in^2 pad area.

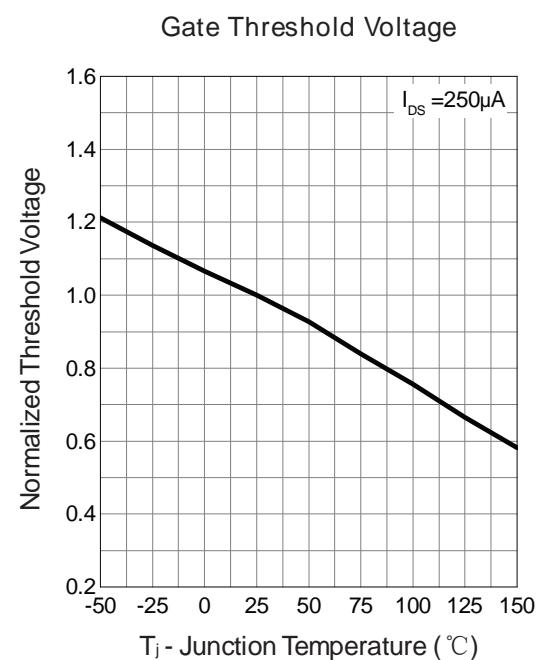
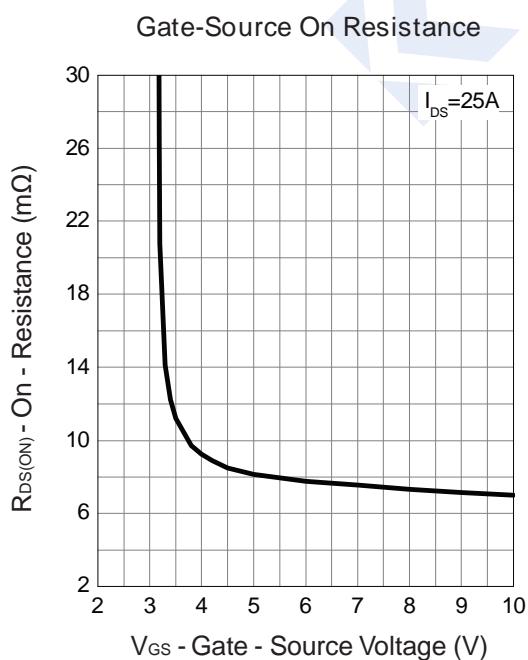
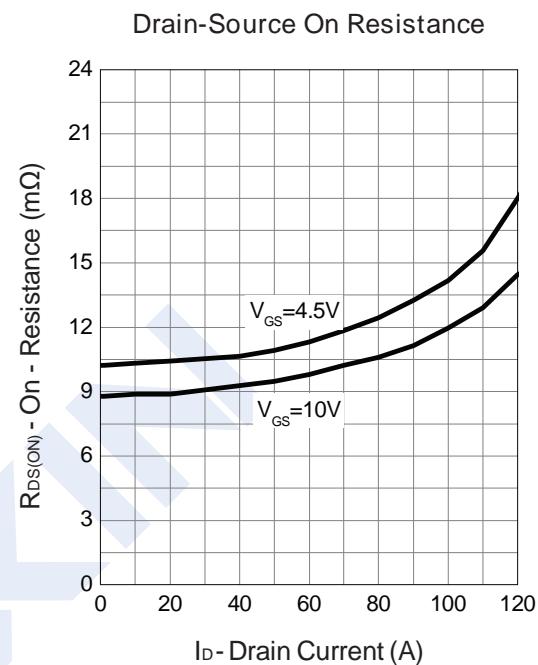
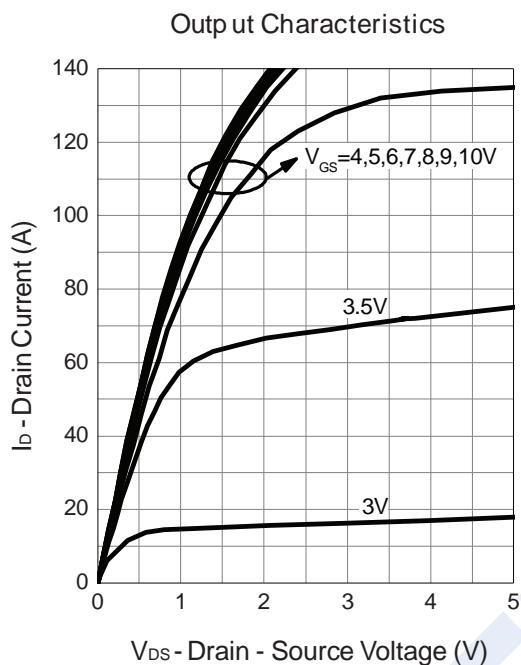
N-Channel MOSFET**2KK5115DFN****■ Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise specified)**

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|--|--------------------------|--|-----|------|-----------|------------------|
| Drain-Source Breakdown Voltage | BV_{DSS} | $I_D = 250 \mu\text{A}, V_{GS} = 0\text{V}$ | 60 | | | V |
| Zero Gate Voltage Drain Current | $I_{DS(on)}$ | $V_{DS} = 48\text{V}, V_{GS} = 0\text{V}$ | | 1 | | μA |
| | | $V_{DS} = 48\text{V}, V_{GS} = 0\text{V}, T_J = 85^\circ\text{C}$ | | 30 | | |
| Gate to Source Leakage Current | I_{GSS} | $V_{DS} = 0\text{V}, V_{GS} = \pm 20\text{V}$ | | | ± 100 | nA |
| Gate to Source Threshold Voltage | $V_{GS(\text{th})}$ | $V_{DS} = V_{GS}, I_D = 250\mu\text{A}$ | 1.1 | | 2.1 | V |
| Static Drain-Source On-Resistance (Note 4) | $R_{DS(on)}$ | $V_{GS} = 10\text{V}, I_D = 25\text{A}$ | | 7.5 | | $\text{m}\Omega$ |
| | | $V_{GS} = 4.5\text{V}, I_D = 25\text{A}$ | | 9.5 | | |
| Input Capacitance | C_{iss} | $V_{GS} = 0\text{V}, V_{DS} = 30\text{V}, f = 1\text{MHz}$ | | 2500 | 3500 | pF |
| Output Capacitance | C_{oss} | | | 215 | | |
| Reverse Transfer Capacitance | C_{rss} | | | 105 | | |
| Gate Resistance | R_g | $V_{GS} = 0\text{V}, V_{DS} = 0\text{V}, f = 1\text{MHz}$ | | 1 | | Ω |
| Total Gate Charge | Q_g | $V_{GS} = 10\text{V}, V_{DS} = 30\text{V}, I_{DS} = 25\text{A}$ | | 45 | 65 | nC |
| Gate Source Charge | Q_{gs} | | | 9 | | |
| Gate Drain Charge | Q_{gd} | | | 8.5 | | |
| Turn-On Delay Time | $t_{d(on)}$ | | | 20 | 36 | |
| Turn-On Rise Time | t_r | $V_{DD}=30\text{V}, R_L=30\Omega, I_{DS}=1\text{A}, V_{GEN}=10\text{V}, R_G=6\Omega$ | | 9 | 16 | ns |
| Turn-Off Delay Time | $t_{d(off)}$ | | | 55 | 99 | |
| Turn-Off Fall Time | t_f | | | 20 | 36 | |
| Body Diode Reverse Recovery Time | t_{rr} | | | 28 | | |
| Body Diode Reverse Recovery Charge | Q_{rr} | $I_F = 25\text{A}, di/dt = 100\text{A}/\mu\text{s}$ | | 30 | | nC |
| Diode Forward Voltage (Note 4) | V_{SD} | | | | 1.3 | V |

Notes 4: Pulse test ; pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$.**■ Marking**

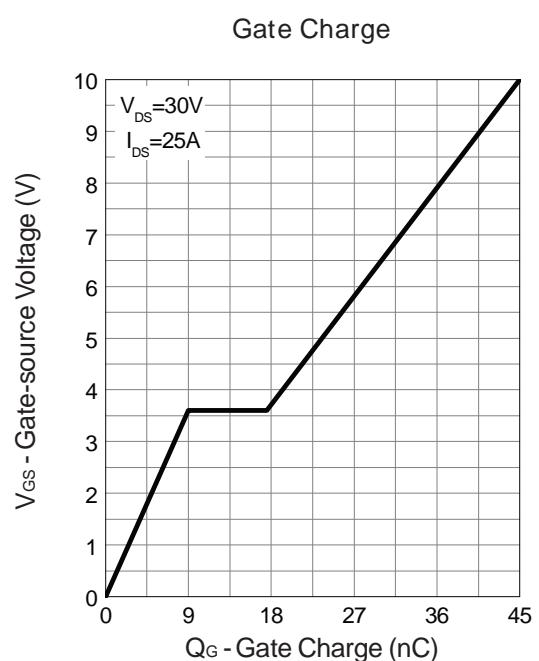
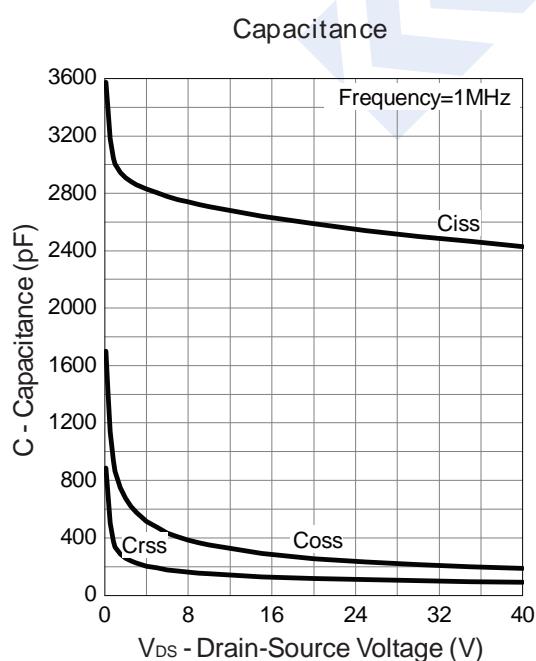
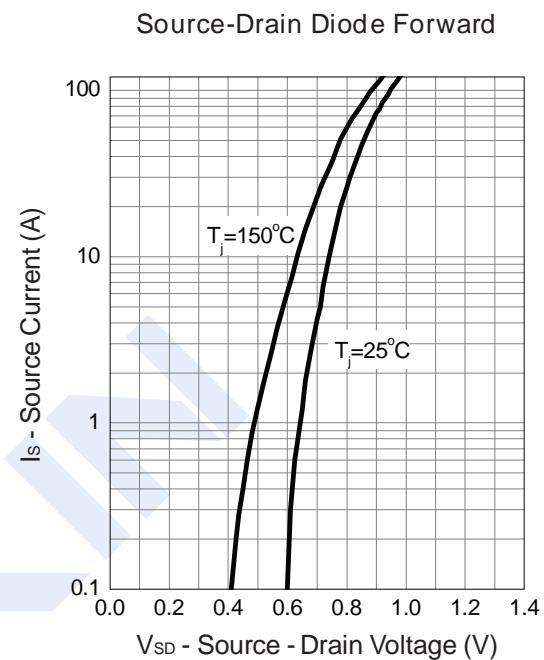
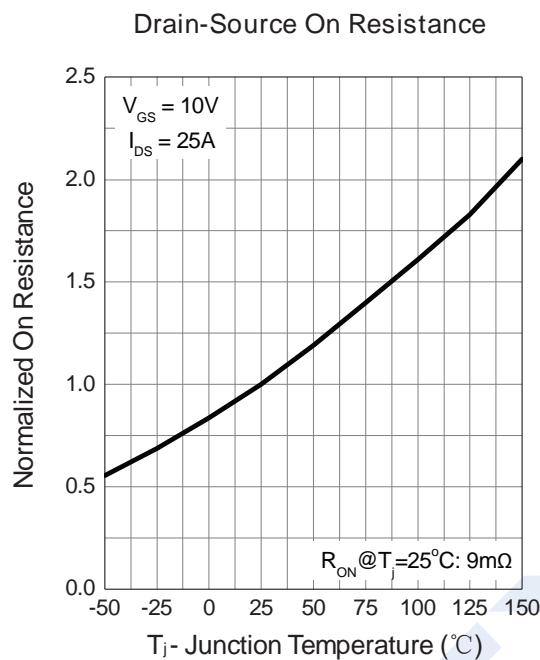
| | |
|---------|----------------|
| Marking | K5115 K**** |
|---------|----------------|

N-Channel MOSFET**2KK5115DFN****■ Typical Characteristics**

N-Channel MOSFET**2KK5115DFN**

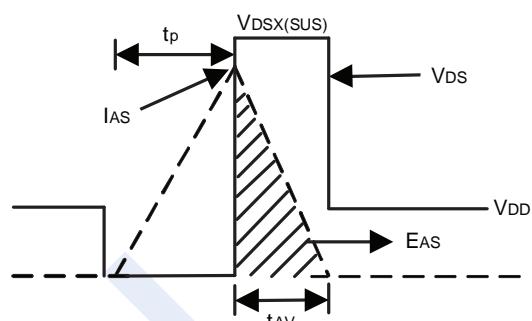
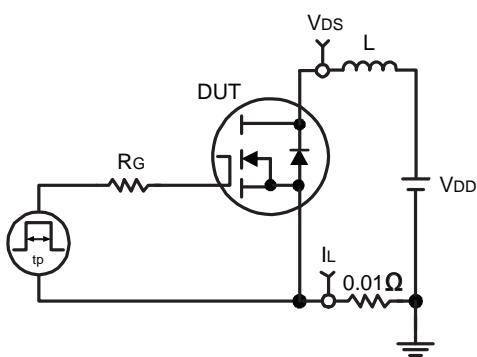
N-Channel MOSFET

2KK5115DFN

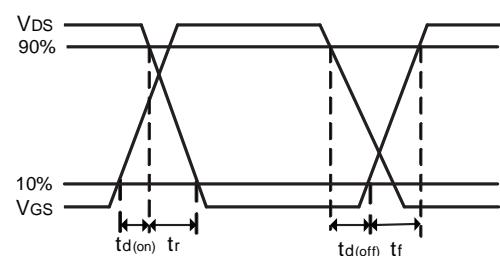
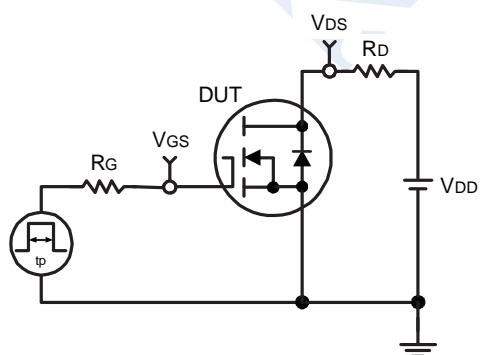


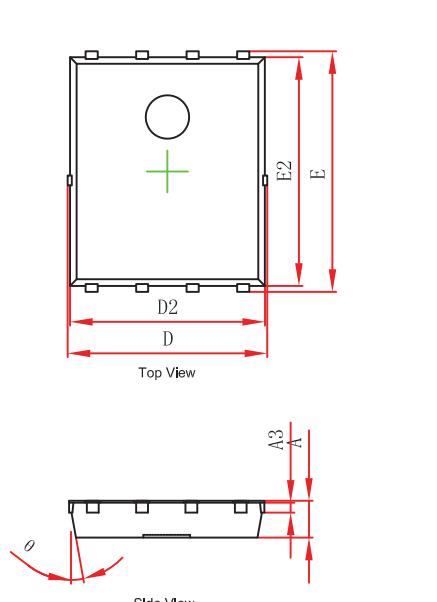
N-Channel MOSFET**2KK5115DFN**

■ Avalanche Test Circuit and Waveforms



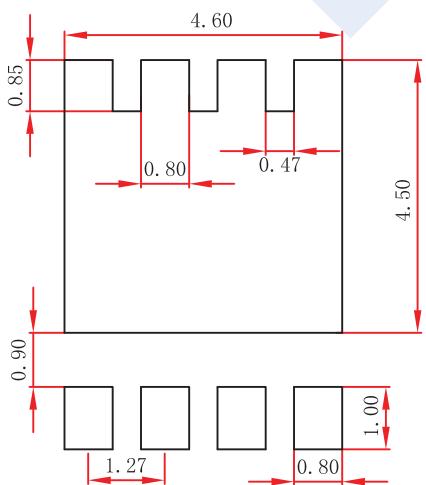
■ Switching Time Test Circuit and Waveforms



N-Channel MOSFET**2KK5115DFN****■ PDFN5x6-8 Package Outline Dimensions**

Bottom View

| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|----------|---------------------------|-----------|----------------------|-----------|
| | Min. | Max. | Min. | Max. |
| A | 0.900 | 1.000 | 0.035 | 0.039 |
| A3 | 0.254REF. | 0.254REF. | 0.010REF. | 0.010REF. |
| D | 4.944 | 5.096 | 0.195 | 0.201 |
| E | 5.974 | 6.126 | 0.235 | 0.241 |
| D1 | 3.910 | 4.110 | 0.154 | 0.162 |
| E1 | 3.375 | 3.575 | 0.133 | 0.141 |
| D2 | 4.824 | 4.976 | 0.190 | 0.196 |
| E2 | 5.674 | 5.826 | 0.223 | 0.229 |
| k | 1.190 | 1.390 | 0.047 | 0.055 |
| b | 0.350 | 0.450 | 0.014 | 0.018 |
| e | 1.270TYP. | 1.270TYP. | 0.050TYP. | 0.050TYP. |
| L | 0.559 | 0.711 | 0.022 | 0.028 |
| L1 | 0.424 | 0.576 | 0.017 | 0.023 |
| H | 0.574 | 0.726 | 0.023 | 0.029 |
| θ | 10° | 12° | 10° | 12° |

■ PDFN5x6-8 Suggested Pad Layout**Note:**

1. Controlling dimension: in millimeters.
2. General tolerance: $\pm 0.05\text{mm}$.
3. The pad layout is for reference purposes only.