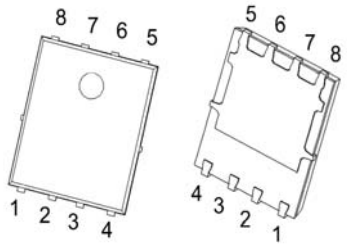
N-Channel MOSFET

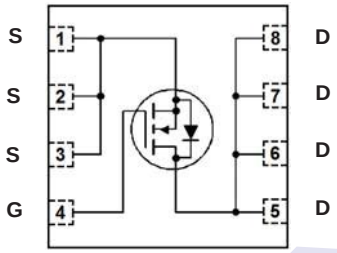
2KK5048DFN

■ Features

- High-speed switching
- Small gate charge
- Low drain-source on-resistance:
  $R_{DS(ON)}$ = 0.9 mΩ (typ.) (V_{GS} = 10 V)
- Low leakage current:
  I_{DSS} = 10 μA (max) (V_{DS} = 30 V)
- Enhancement mode

PDFN5x6-8





■ Absolute Maximum Ratings (T_a = 25℃ unless otherwise noted)

Parameter		Symbol	Rating	Unit
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	Silicon limit,Note 1,2	I_D	150	A
	T_C=25℃,Note 1		60	
Pulsed Drain Current	t = 1 ms,Note 1	I_{DP}	200	
Single-pulse Avalanche Energy	Note 5	E_{AS}	355	mJ
Avalanche Current		I_{AR}	60	A
Power Dissipation	T_C=25℃	P_D	64	W
	t=10s,Note 3		2.8	
	t=10s,Note 4		1.6	
Channel-to-case Thermal Resistance	T_C=25℃	$R_{th(ch-c)}$	1.95	℃/W
Channel-to-ambient Thermal Resistance	t=10s,Note 3	$R_{th(ch-a)}$	44.6	
Channel-to-ambient Thermal Resistance	t=10s,Note 4		78.1	
Channel Temperature		T_{ch}	150	℃
Storage Temperature Range		T_{stg}	-55 to 150	

Note 1: Ensure that the channel temperature does not exceed 150℃.

Note 2: Limited by silicon chip capability. Package limit is 60 A.

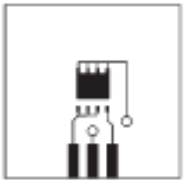
Note 3: Device mounted on a glass-epoxy board (a)

Note 4: Device mounted on a glass-epoxy board (b)

Note 5: V_{DD} = 24 V, T_{ch} = 25℃(initial), L = 76 μH, I_{AR} = 60 A

FR-4
25.4 × 25.4 × 0.8
(Unit: mm)

Device Mounted on a Glass-Epoxy Board (a)



FR-4
25.4 × 25.4 × 0.8
(Unit: mm)

Device Mounted on a Glass-Epoxy Board (b)

N-Channel MOSFET

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■ Electrical Characteristics (T_a = 25℃ unless othewise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 10 mA, V_{GS} = 0V	30			V
	BV_{DSX}	I_D = 10 mA, V_{GS} = -20V	15			
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V			10	μA
Gate to Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Gate to Source Threshold Voltage	V_{th}	V_{DS} = 10 V, I_D = 0.5 mA	1.3		2.3	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 30 A		0.9	1.4	mΩ
		V_{GS} = 4.5 V, I_D = 30 A			2.1	
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 15 V, f = 1 MHz		3400	4400	pF
Output Capacitance	C_{oss}			1800		
Reverse Transfer Capacitance	C_{rss}			93	200	
Gate Resistance	R_g			1.1	1.7	Ω
Total Gate Charge	Q_g	V_{DD} ≈ 15 V, V_{GS} = 10V, I_D = 60 A		46		nC
Total Gate Charge		V_{DD} ≈ 15 V, V_{GS} = 4.5V, I_D = 60 A		20		
Gate Source Charge 1	Q_{gs1}	V_{DD} ≈ 15 V, V_{GS} = 10V, I_D = 60 A		12.1		
Gate Drain Charge	Q_{gd}			4.3		
Gate Switch Charge	Q_{SW}			10.6		
Turn-On DelayTime	$t_{d(on)}$	V_{GS} = 10V, VDD ≈ 15 V, R_L = 0.5 Ω, R_{GEN} = 4.7 Ω		16		ns
Turn-On Rise Time	t_r			5.6		
Turn-Off DelayTime	$t_{d(off)}$			50		
Turn-Off Fall Time	t_f			8.9		
Body Diode Reverse Recovery Time	t_{rr}	I_F = 20 A, dI/dt = 500 A/μs		12.6		
Body Diode Reverse Recovery Charge	Q_{rr}			15.2		nC
Maximum Body-Diode Continuous Current	I_S				200	A
Diode Forward Voltage	V_{SD}	V_{GS} = 0 V, I_S = 60 A			1.2	V

Note 6: Ensure that the channel temperature does not exceed 150℃.

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■ Typical Characterisitics

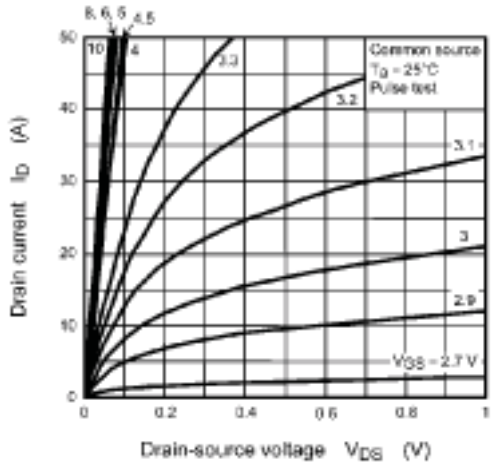

Fig. 1 I_D - V_{DS}

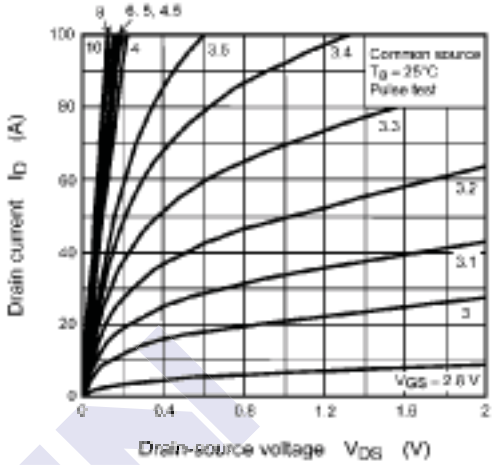

Fig. 2 I_D - V_{DS}

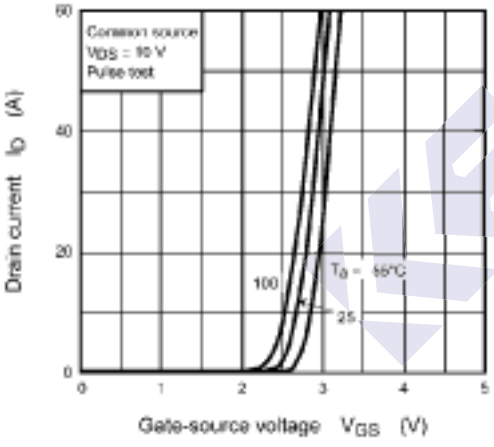

Fig. 3 I_D - V_{GS}

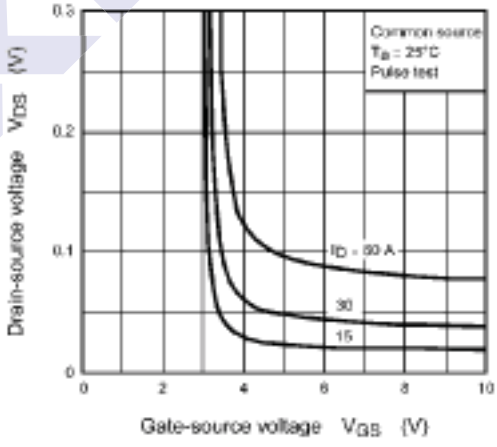

Fig. 4 V_{DS} - V_{GS}

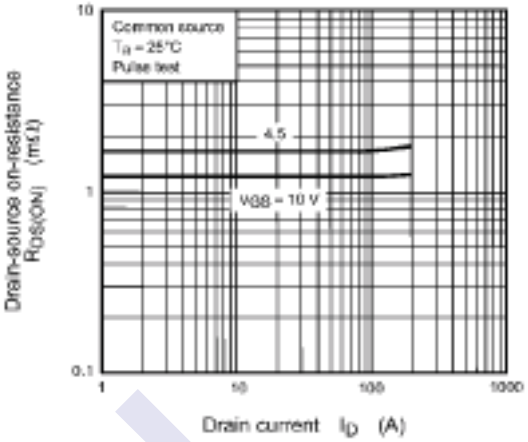

Fig. 5 $R_{DS(ON)}$ - I_D

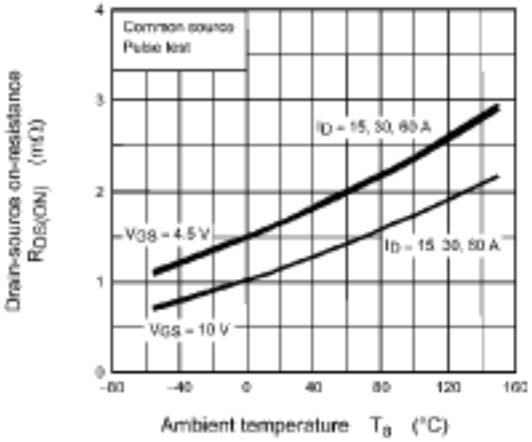

Fig. 6 $R_{DS(ON)}$ - T_a

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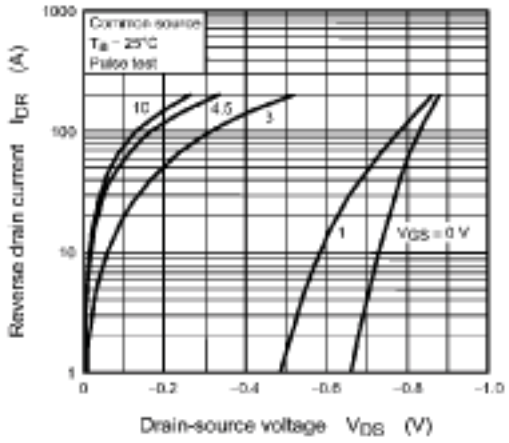

Fig. 7 I_{DR} - V_{DS}

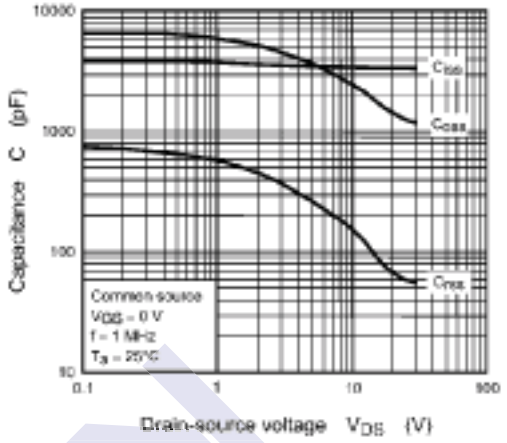

Fig. 8 Capacitance - V_{DS}

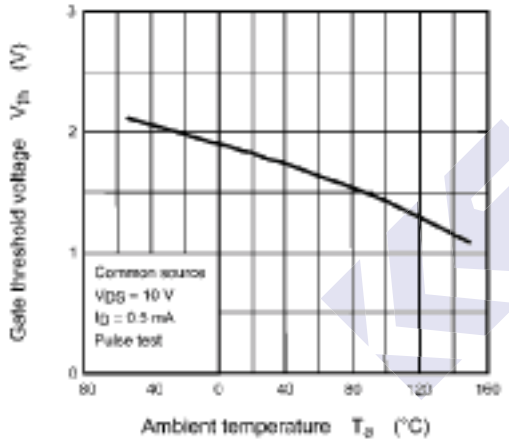

Fig. 9 V_{th} - T_a

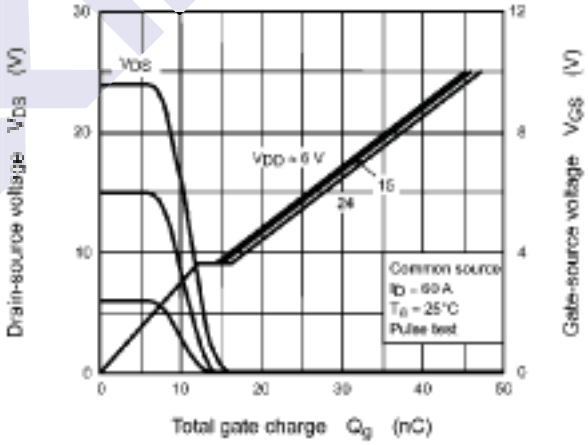

Fig. 10 Dynamic Input/Output Characteristics

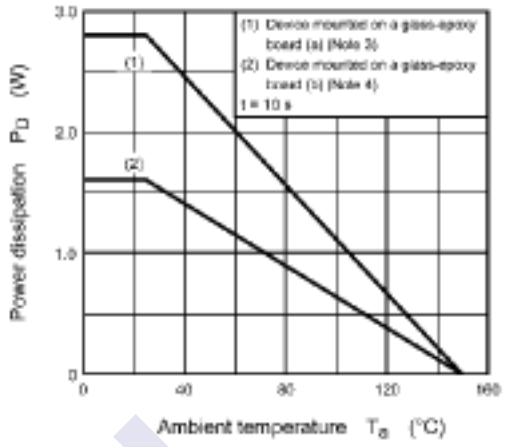

Fig. 11 P_D - T_a(Guaranteed Maximum)

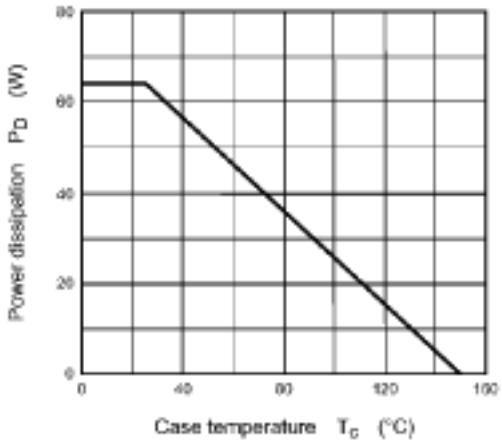

Fig. 12 P_D - T_c(Guaranteed Maximum)

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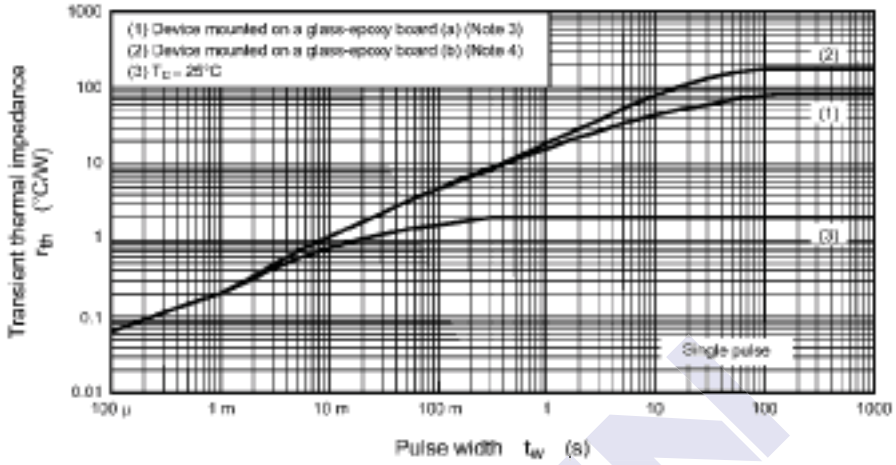

Fig. 13 r_{th} - t_w(Guaranteed Maximum)

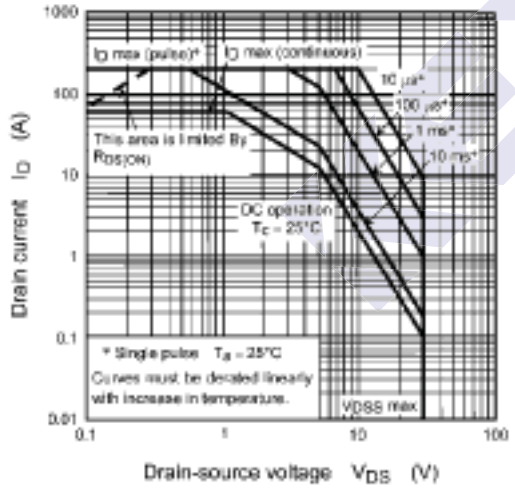

Fig. 14 Safe Operating Area(Guaranteed Maximum)

N-Channel MOSFET

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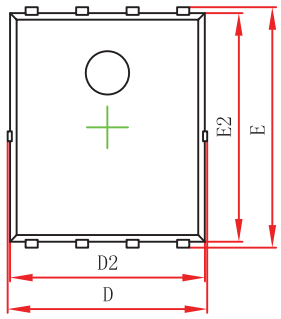
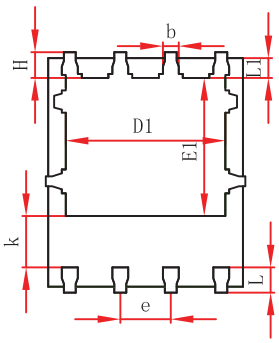
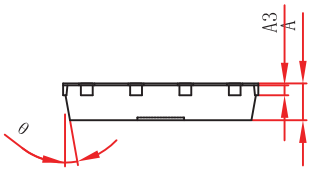
■ PDFN5x6-8 Package Outline Dimensions



Top View



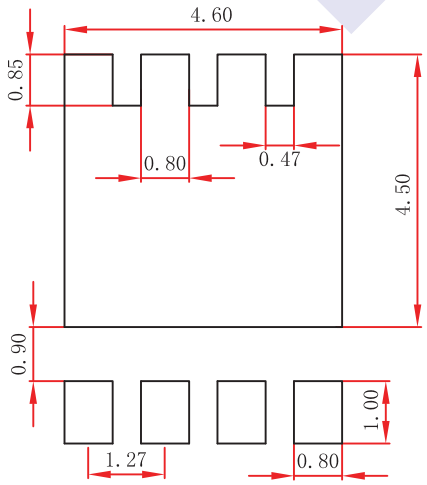
Bottom View



Side View

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.000	0.035	0.039
A3	0.254REF.		0.010REF.	
D	4.944	5.096	0.195	0.201
E	5.974	6.126	0.235	0.241
D1	3.910	4.110	0.154	0.162
E1	3.375	3.575	0.133	0.141
D2	4.824	4.976	0.190	0.196
E2	5.674	5.826	0.223	0.229
k	1.190	1.390	0.047	0.055
b	0.350	0.450	0.014	0.018
e	1.270TYP.		0.050TYP.	
L	0.559	0.711	0.022	0.028
L1	0.424	0.576	0.017	0.023
H	0.574	0.726	0.023	0.029
θ	10°	12°	10°	12°

■ PDFN5x6-8 Suggested Pad Layout



Note:

1.Controlling dimension:in millimeters.
2.General tolerance:±0.05mm.
3.The pad layout is for reference purposes only.