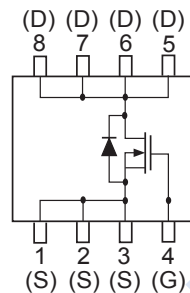


## N-Channel MOSFET

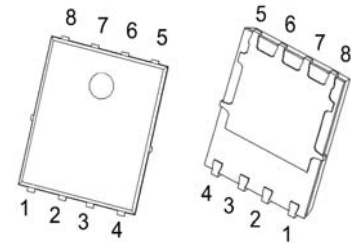
## 2KK5035DFN

## ■ Features

- $V_{DS}$  (V) = 150V
- $I_D$  = 30 A
- $R_{DS(ON)} \leq 38m\Omega$  ( $V_{GS} = 10V$ )



DFN5x6-8(PDFNWB5x6-8L)

■ Absolute Maximum Ratings ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	$V_{DS}$	150	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current ( $T_J=150^\circ\text{C}$ )	$I_D$	$T_C=25^\circ\text{C}$	30 <sup>a</sup>
		$T_C=70^\circ\text{C}$	26
		$T_A=25^\circ\text{C}$	7.7 <sup>b,c</sup>
		$T_A=70^\circ\text{C}$	6.2 <sup>b,c</sup>
Pulsed Drain Current	$I_{DM}$	60	A
Continuous Source-Drain Diode Current	$I_S$	$T_C=25^\circ\text{C}$	30 <sup>a</sup>
		$T_A=25^\circ\text{C}$	4.5 <sup>b,c</sup>
Single Pulse Avalanche Current	$L=0.1\text{mH}$	$I_{AS}$	30
Single Pulse Avalanche Energy			$E_{AS}$
Maximum Power Dissipation	$P_D$	$T_C=25^\circ\text{C}$	96
		$T_C=70^\circ\text{C}$	62
		$T_A=25^\circ\text{C}$	5.4 <sup>b,c</sup>
		$T_A=70^\circ\text{C}$	3.5 <sup>b,c</sup>
Thermal Resistance.Junction- to-Ambient <sup>b,f</sup>	$t \leq 10\text{s}$	$R_{thJA}$	23
Thermal Resistance.Junction- to-Case (Drain)	Steady state	$R_{thJC}$	1.3
Soldering Recommendations (Peak Temperature) <sup>d,e</sup>			260
Junction Temperature	$T_J$	150	$^\circ\text{C}$
Storage Temperature Range	$T_{stg}$	-55 to 150	$^\circ\text{C}$

Notes: a.Package limited. b.Surface Mounted on 1" x 1" FR4 board. c.t = 10 s.

d.The DFN5X6-8 is a leadless package. The end of the lead terminal is exposed copper(not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed to ensure adequate bottom side solder interconnection.

e.Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

f.Maximum under Steady State conditions is 65  $^\circ\text{C}/\text{W}$ .

## N-Channel MOSFET

## 2KK5035DFN

■ Electrical Characteristics (T<sub>J</sub> = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V <sub>DSS</sub>	I <sub>D</sub> =250μA, V <sub>GS</sub> =0V	150			V
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	I <sub>D</sub> =250μA		200		mV/°C
V <sub>GS(th)</sub> Temperature Coefficient	ΔV <sub>GS(th)</sub> /T <sub>J</sub>			-10		
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =150V, V <sub>GS</sub> =0V			1	μA
		V <sub>DS</sub> =150V, V <sub>GS</sub> =0V, T <sub>C</sub> =55°C			10	
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> =0V, V <sub>GS</sub> =±20V			±100	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	2		4	V
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≥5V, V <sub>GS</sub> =10V	30			A
Static Drain-Source On-Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =7.7A			38	mΩ
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> =15V, I <sub>D</sub> =7.7A		22		S
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> =0V, V <sub>DS</sub> =75V, f=1MHz		2100		pF
Output Capacitance	C <sub>oss</sub>			160		
Reverse Transfer Capacitance	C <sub>rss</sub>			45		
Turn-On DelayTime	t <sub>d(on)</sub>	V <sub>DD</sub> =75V, R <sub>L</sub> =12Ω, I <sub>D</sub> =6.2A, V <sub>GEN</sub> =10V, R <sub>g</sub> =1Ω		15	25	ns
Turn-On Rise Time	t <sub>r</sub>			10	15	
Turn-Off DelayTime	t <sub>d(off)</sub>			25	40	
Turn-Off Fall Time	t <sub>f</sub>			10	15	
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =75V, I <sub>D</sub> =7.7A, V <sub>GS</sub> =10V		35	53	nC
Gate Source Charge	Q <sub>gs</sub>			8		
Gate Drain Charge	Q <sub>gd</sub>			9		
Body Diode Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 6.2A, di/dt = 100A/μs, T <sub>J</sub> =25°C		75	115	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>			245	370	nC
Body Diode Reverse Recovery Fall Time	t <sub>a</sub>			58		ns
Body Diode Reverse Recovery Rise Time	t <sub>b</sub>			17		
Maximum Body-Diode Continuous Current	I <sub>S</sub>	T <sub>C</sub> =25°C			30	A
Maximum Body-Diode Current ( Pulsed )	I <sub>SM</sub>				30	
Diode Forward Voltage	V <sub>SD</sub>	I <sub>SD</sub> =6.2A, V <sub>GS</sub> =0V			1.2	V

Notes: a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%

b. Guaranteed by design, not subject to production testing.

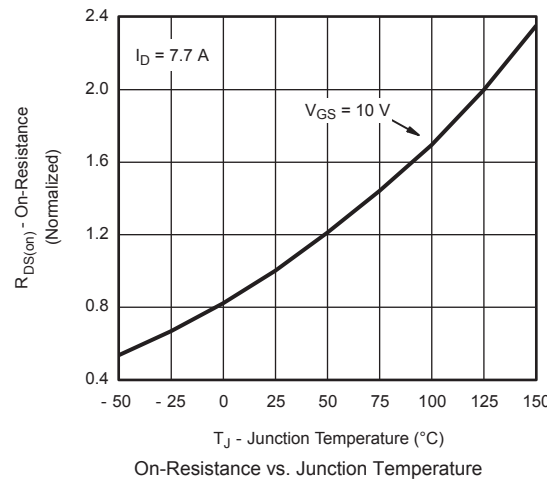
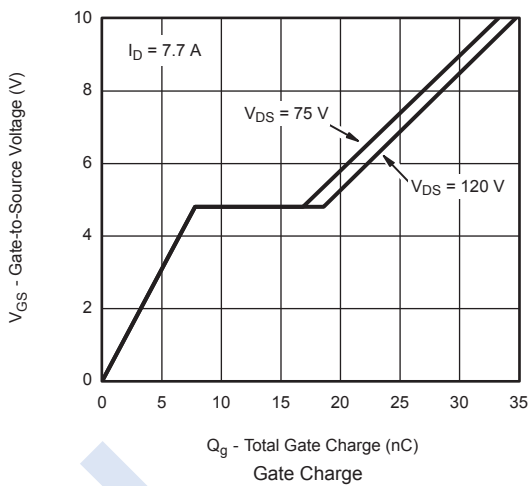
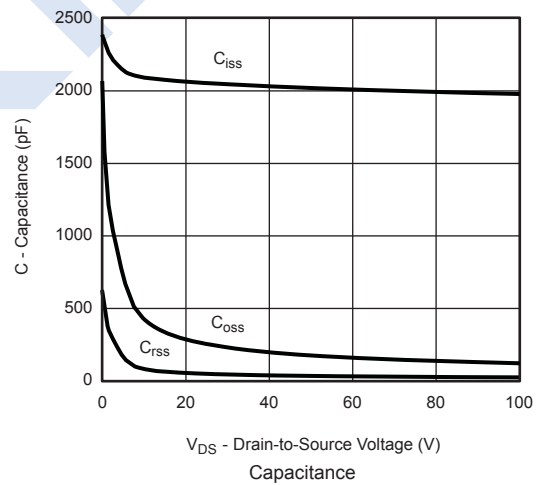
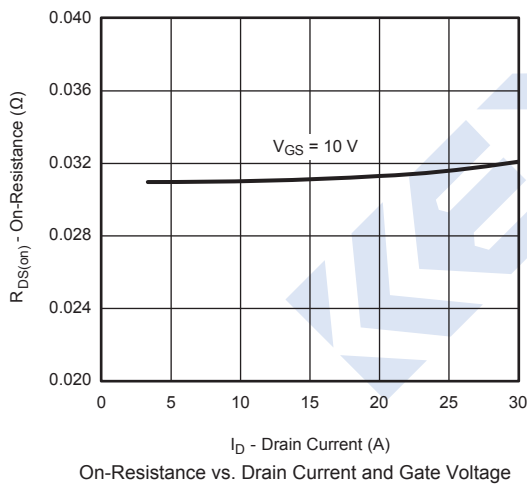
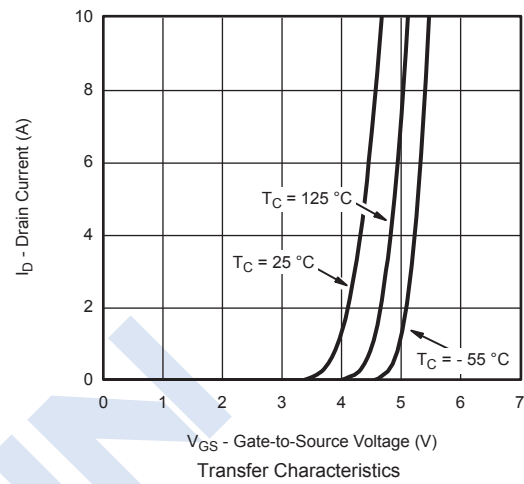
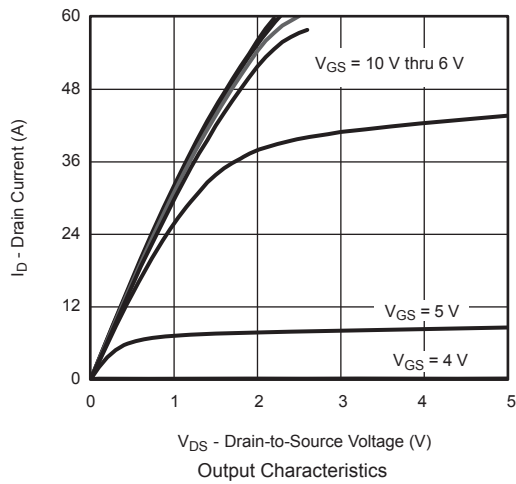
## ■ Marking

Marking	K5035 KC****
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# N-Channel MOSFET

## 2KK5035DFN

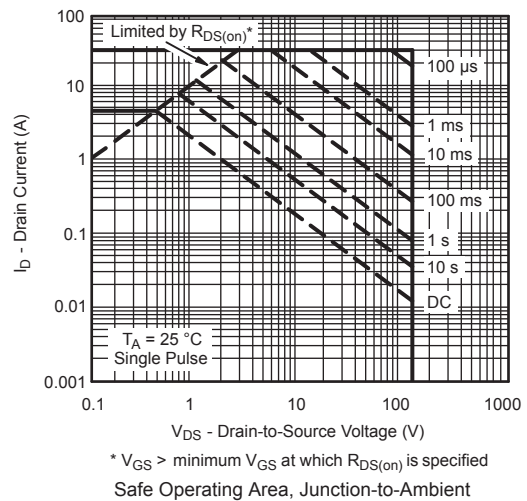
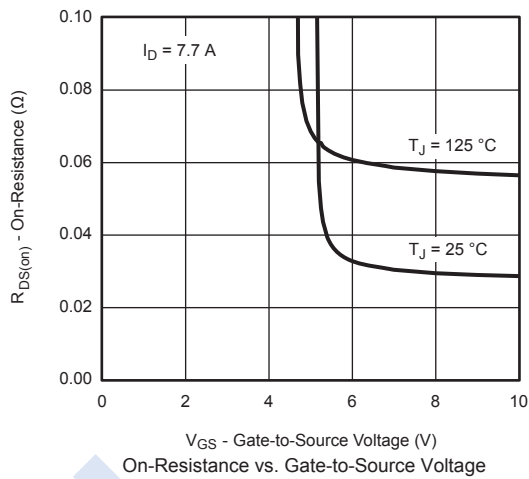
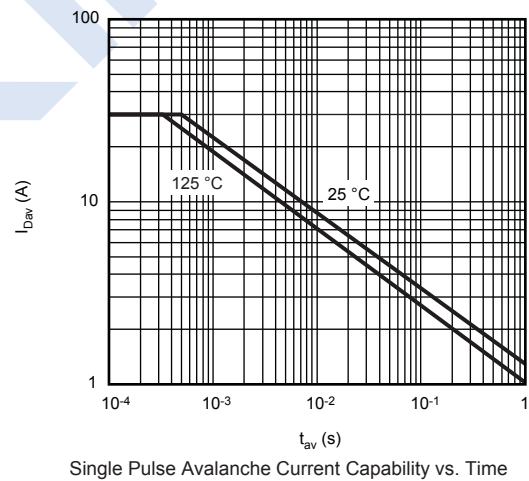
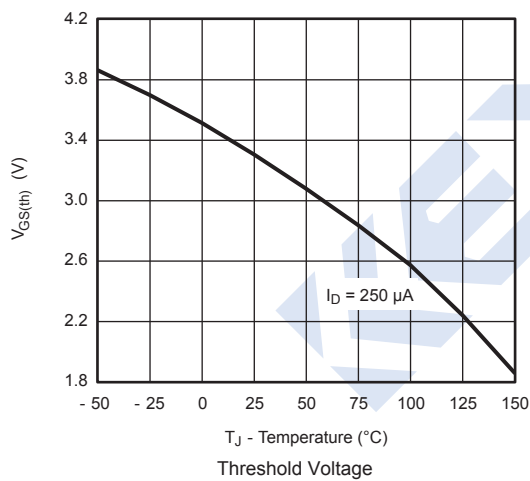
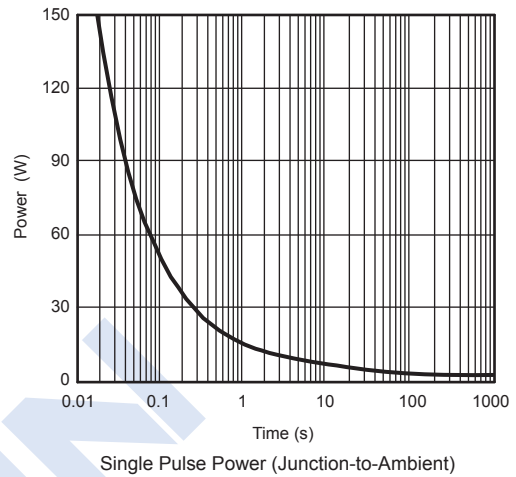
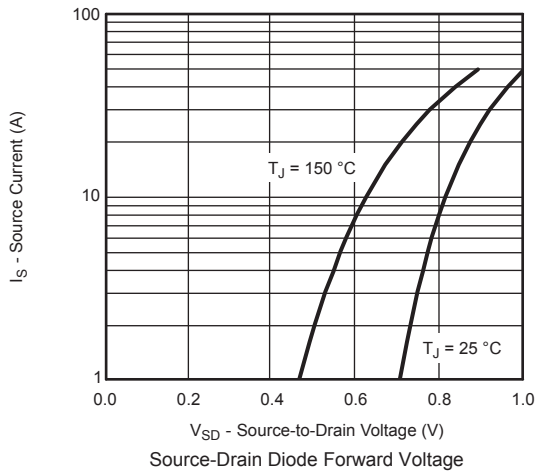
■ Typical Characteristics 25°C unless otherwise noted



# N-Channel MOSFET

## 2KK5035DFN

■ Typical Characteristics 25°C unless otherwise noted

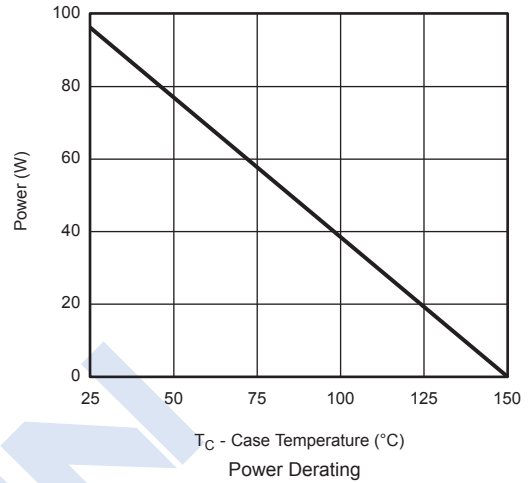
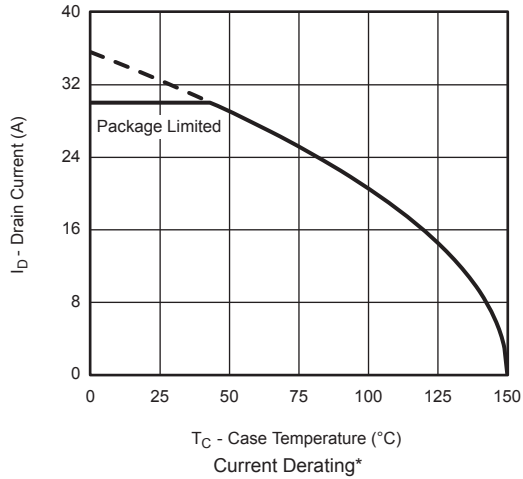


\*  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified  
Safe Operating Area, Junction-to-Ambient

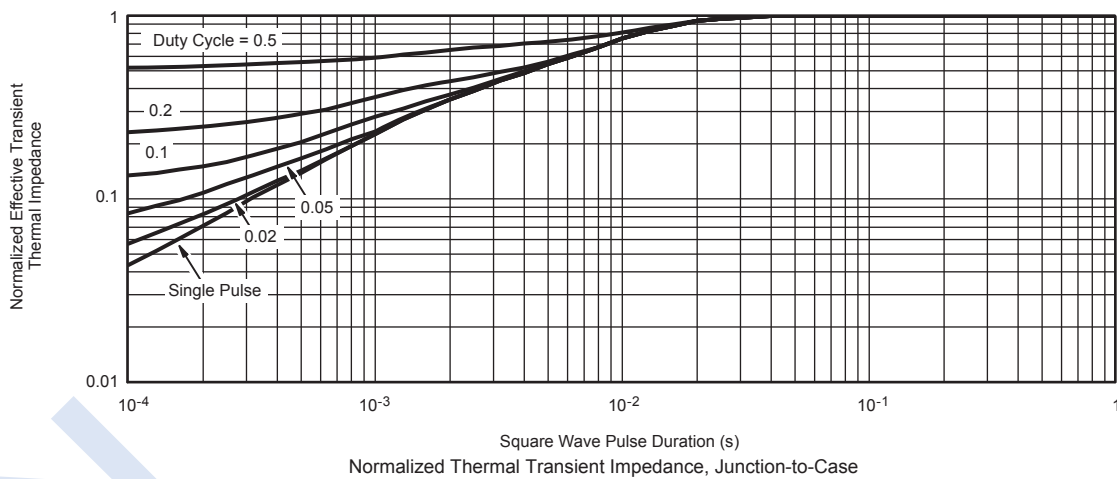
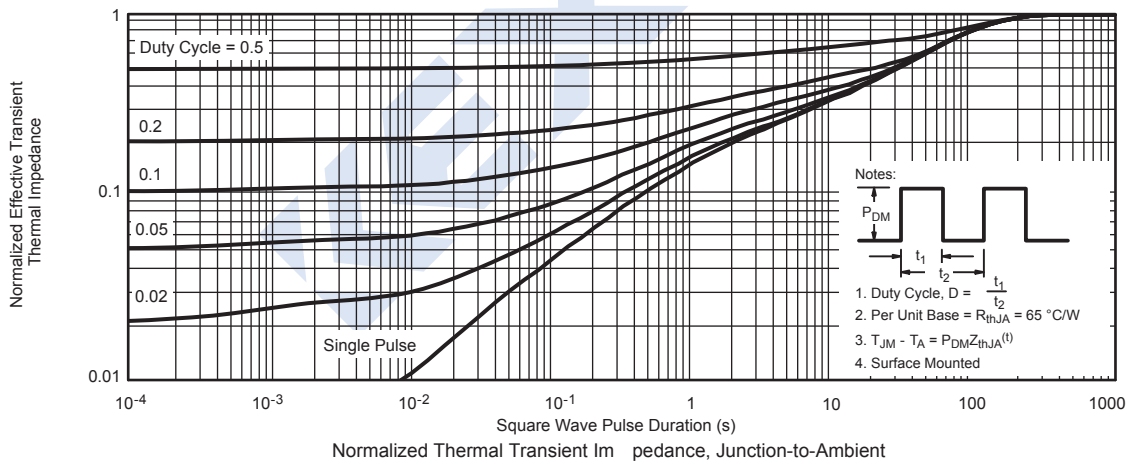
# N-Channel MOSFET

## 2KK5035DFN

■ Typical Characteristics 25°C unless otherwise noted



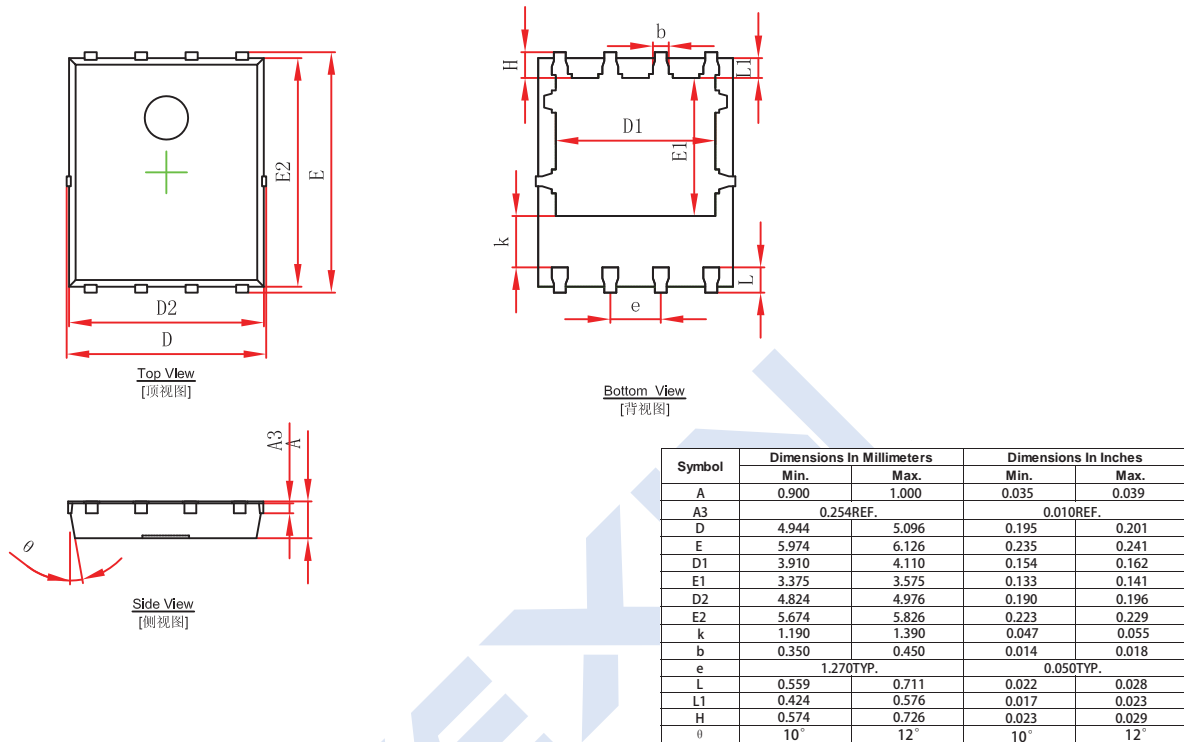
\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 150\text{ }^\circ\text{C}$ , using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



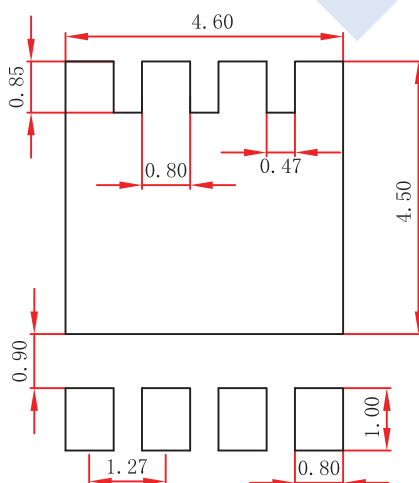
## N-Channel MOSFET

## 2KK5035DFN

## ■ DFN5x6-8(PDFNWB5x6-8L) Package Outline Dimensions



## ■ DFN5x6-8(PDFNWB5x6-8L) Suggested Pad Layout



## Note:

1. Controlling dimension: in millimeters.
2. General tolerance:  $\pm 0.05$ mm.
3. The pad layout is for reference purposes only.