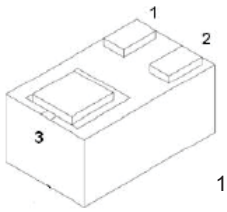
P-Channel MOSFET

2KJ7112DFN

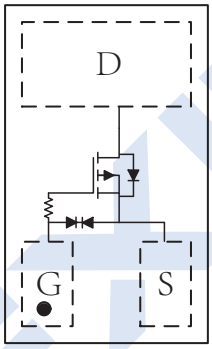
DFN1006-3



1.GATE
2.SOURCE
3.DRAIN

■ Features

- $V_{DS\ (V)}$ = -30 V
- I_D = -0.57 A
- $R_{DS(ON)}$ (at V_{GS} = -4.5 V) = 415 mΩ
- $R_{DS(ON)}$ (at V_{GS} = -2.5 V) = 500 mΩ
- $R_{DS(ON)}$ (at V_{GS} = -1.8 V) = 600 mΩ
- ESD Protected



■ Absolute Maximum Ratings (T_a = 25℃ unless otherwise noted)

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	±10	
Continuous Drain Current (Note 1)	I_D	-0.57	A
Pulsed Drain Current (tp=10μs)	I_{DM}	-1.1	
Power Dissipation (Note 1)	P_D	0.25	W
Thermal Resistance, Junction-to-Ambient (Note 1)	$R_{\theta JA}$	500	℃/W
Junction Temperature	T_J	150	℃
Storage Temperature Range	T_{stg}	-55 to 150	

Note 1.Surface mounted on FR4 board using the minimum recommended pad size.

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■ Electrical Characteristics (T_a = 25℃ unless othewise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
STATIC PARAMETERS						
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = -250 μA, V_{GS} = 0V	-30			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -24 V, V_{GS} = 0 V			-1	μA
Gate to Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±10 V			±5	
Gate to Source Threshold Voltage (Note 2)	$V_{GS(th)}$	V_{DS} = V_{GS} , I_D = -250μA	-0.45		-1.0	V
Static Drain-Source On-Resistance (Note 2)	$R_{DS(ON)}$	V_{GS} = -4.5 V, I_D = -0.2 A		415	650	mΩ
		V_{GS} = -2.5 V, I_D = -0.1 A		500	800	
		V_{GS} = -1.8 V, I_D = -75 mA		600	950	
Diode Forward Voltage	V_{SD}	V_{GS} = 0 V, I_S = -0.3 A			-1.2	V
DYNAMIC PARAMETERS (Note 4)						
Input Capacitance	C_{iss}	V_{GS} = 0 V, f = 1 MHz, V_{DS} = -15 V,		110		pF
Output Capacitance	C_{oss}			18		
Reverse Transfer Capacitance	C_{rss}			11		
Total Gate Charge	$Q_{g(tot)}$	V_{GS} = -4.5V, V_{DS} = -15 V, I_D = -0.5 A		1.45		nC
Threshold Gate Charge	$Q_{g(th)}$			0.46		
Gate Source Charge	Q_{gs}			0.6		
Gate Drain Charge	Q_{gd}			0.44		
SWITCHING PARAMETERS (Note 4)						
Turn-On DelayTime (Note 3)	$t_{d(on)}$	V_{GS} = -4.5V, V_{DD} = -15 V, I_D = -500mA, R_G = 1 Ω		8		ns
Turn-On Rise Time (Note 3)	t_r			6		
Turn-Off DelayTime (Note 3)	$t_{d(off)}$			26		
Turn-Off Fall Time (Note 3)	t_f			4		

Notes:

2. Pulse Test : Pulse width=300μs, duty cycle≤2%.
3. Switching characteristics are independent of operating junction temperatures.
4. Graranted by design，not subject to producting.

■ Marking

Marking	3

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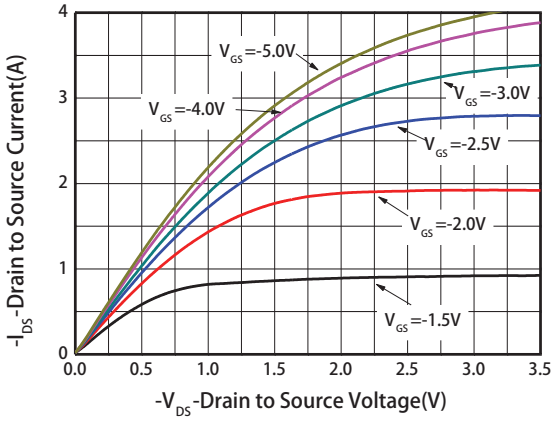
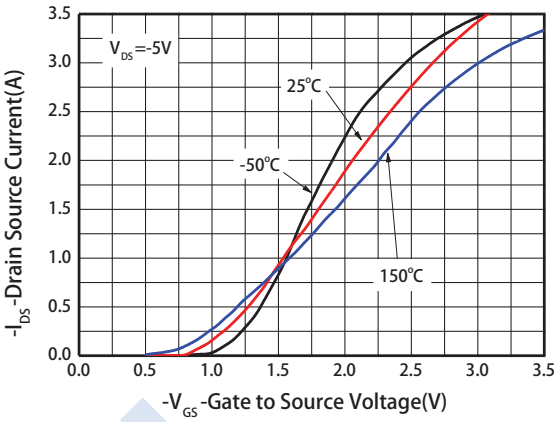
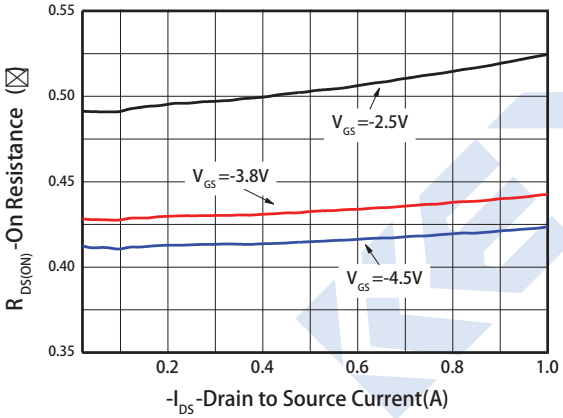
■ Typical Characterisitics



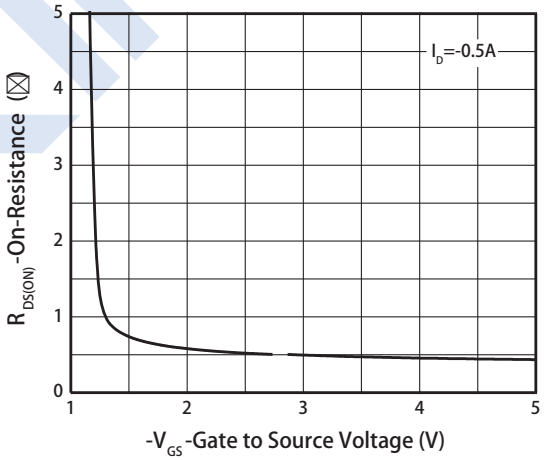
Output characteristics



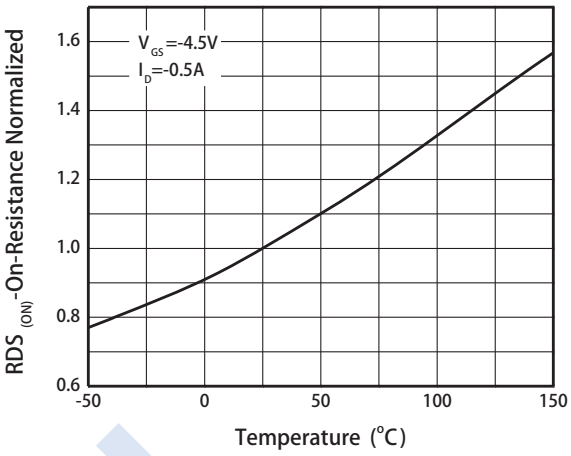
Transfer characteristics



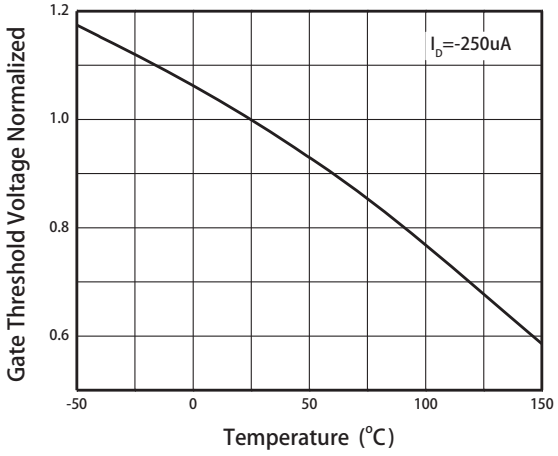
On-Resistance vs. Drain current



On-Resistance vs. Gate-to-source voltage



On-Resistance vs. Junction temperature



Threshold voltage vs. Temperature

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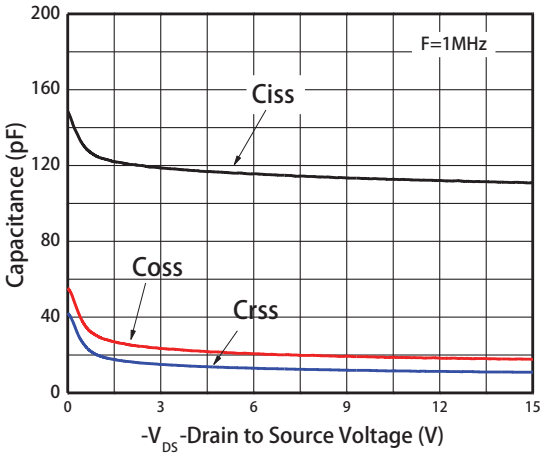
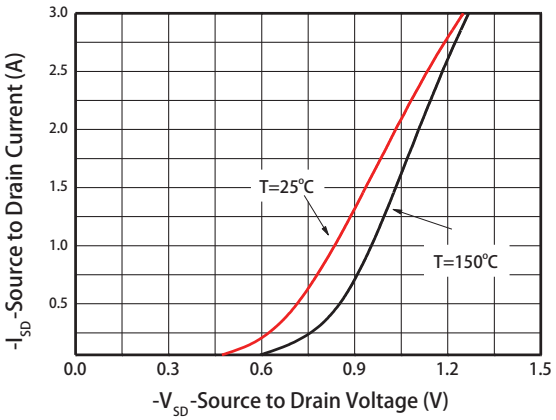
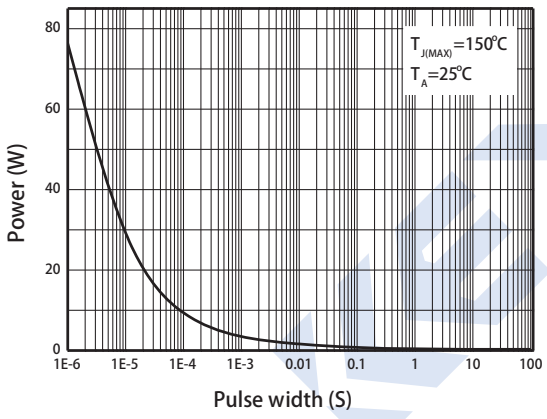


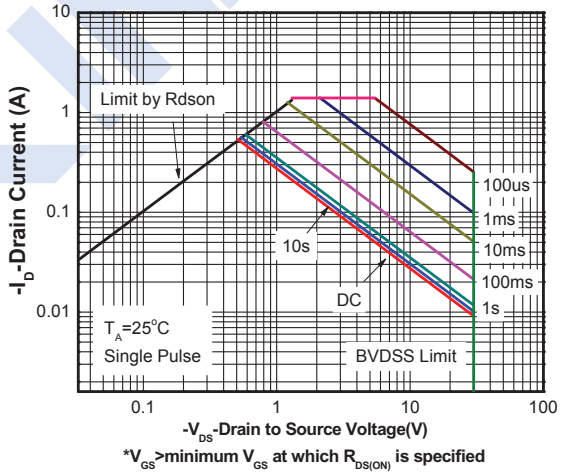
Capacitance



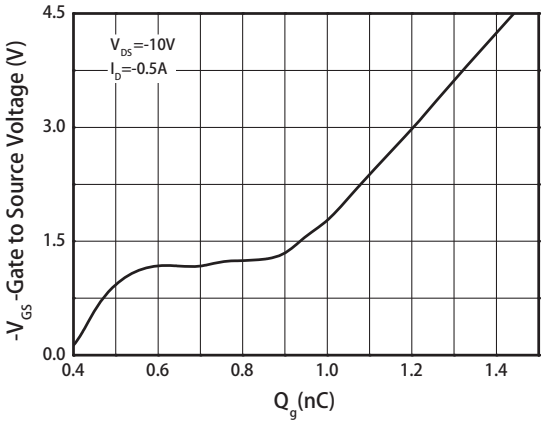
Body diode forward voltage



Single pulse power



Safe operating power



Gate Charge Characteristics

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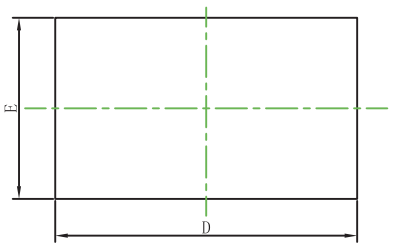
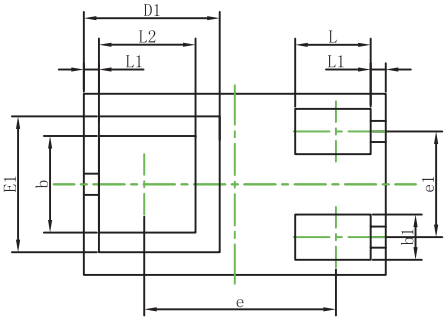
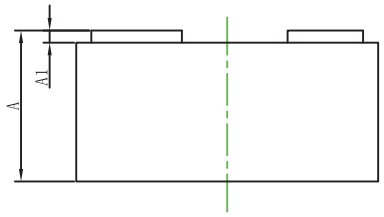
■ DFN1006-3 Package Outline Dimensions



TOP VIEW



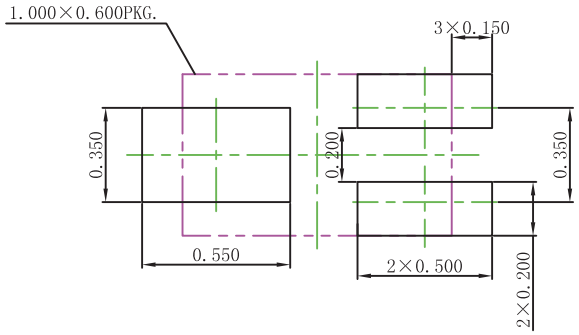
BOTTOM VIEW



SIDE VIEW

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.450	0.550	0.018	0.022
A1	0.010	0.100	0.000	0.004
D	0.950	1.050	0.037	0.041
E	0.550	0.650	0.022	0.026
D1	0.450REF.		0.018REF.	
E1	0.450REF.		0.018REF.	
b	0.270	0.370	0.011	0.015
b1	0.100	0.200	0.004	0.008
e	0.635REF.		0.025REF.	
e1	0.300	0.400	0.012	0.016
L	0.200	0.300	0.008	0.012
L1	0.050REF.		0.002REF.	
L2	0.270	0.370	0.011	0.015

■ DFN1006-3 Suggested Pad Layout



Note:
1.Controlling dimension:in millimeters.
2.General tolerance:± 0.050mm.
3.The pad layout is for reference purposes only.